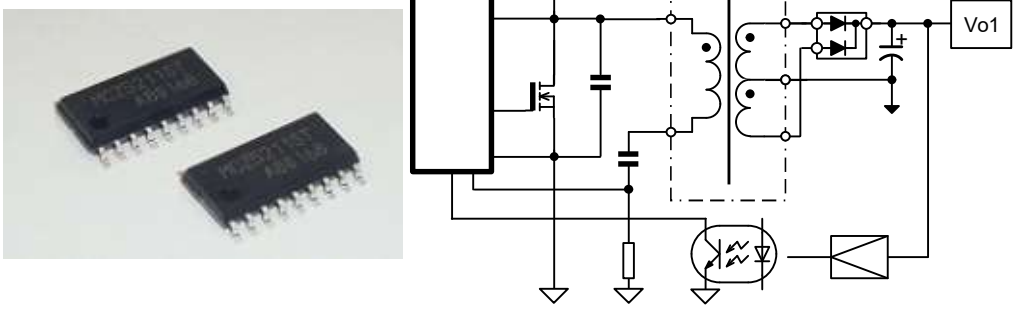
LLC Current Resonance
Bridge Converter Control IC
with Standby-compatible Self-Startup Pin

MCZ5211ST



Application Note Version 1.0

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1 Overview

The MCZ5211ST is a frequency modulation type current resonance power supply control IC.

It features a self-startup pin (drain kick function) with a high withstand voltage of 600 V for loss-free startup. It also includes a high-withstand-voltage gate driver enabling direct drive of high-side MOSFETs. Various protection functions are also included, such as overcurrent protection and out-of-resonance protection (capacitive mode protection), enabling the number of components to be reduced and efficiency increased.

Standby power improvement functions are provided (active standby function and burst function) to make it possible to maintain the power supply with high efficiency across the entire load range, making it ideal for use with the following products:

- LED/OLED large flat-screen TV power supplies
- Laser printer and other office equipment power supplies
- External power supplies such as AC adapters
- Industrial machinery power supplies
- Isolated LED lighting power supplies
- Audio and projector power supplies

1.1 Features

1. 600 V withstand voltage self-startup pin for loss-free startup ***NEW***
2. High-reliability 600 V withstand-voltage gate driver enabling direct drive of high-side MOSFETs
3. Various protection functions required for LLC converters (overcurrent, timer latch, undervoltage, overheat protection)
4. Overcurrent protection function based on direct detection of resonance current in both positive and negative directions
5. Capacitive mode protection function based on direct detection of resonance current in both positive and negative directions
6. Support for a wide range of input voltages with 35 V Vc1 withstand voltage (Vc2 UVLO 10 V/7.5 V typ.)
7. MOSFET drive power supply regulator (Vc2) to ensure stable drive
8. Independent separate voltage drop protection functions (UVLO) for high-side and low-side gate outputs
9. Soft start function to reduce MOSFET di/dt stress
10. Safety protection function to stop operation during low input voltage operation such as brown outs
11. Input voltage correction function in the frequency clamp type overcurrent protection function (OCP2) corresponding to peak load, reducing stress during overloads by reducing the dependency of the overcurrent protection operation start point on the input voltage ***NEW***
12. Two-stage switching of timer charging current during OCP2 operation to ensure safe operation at peak load for several 100 ms and safety protection for the maximum peak load
13. Active standby function to improve efficiency at light load
14. High-efficiency burst function to improve efficiency during standby load
15. Immediate latch stop function (SST pin) using external signal
16. Vc1 OVP function (immediate latch stop) ***NEW***
17. Support for 500 kHz operation with control suited for higher frequencies

1.2 Block diagram

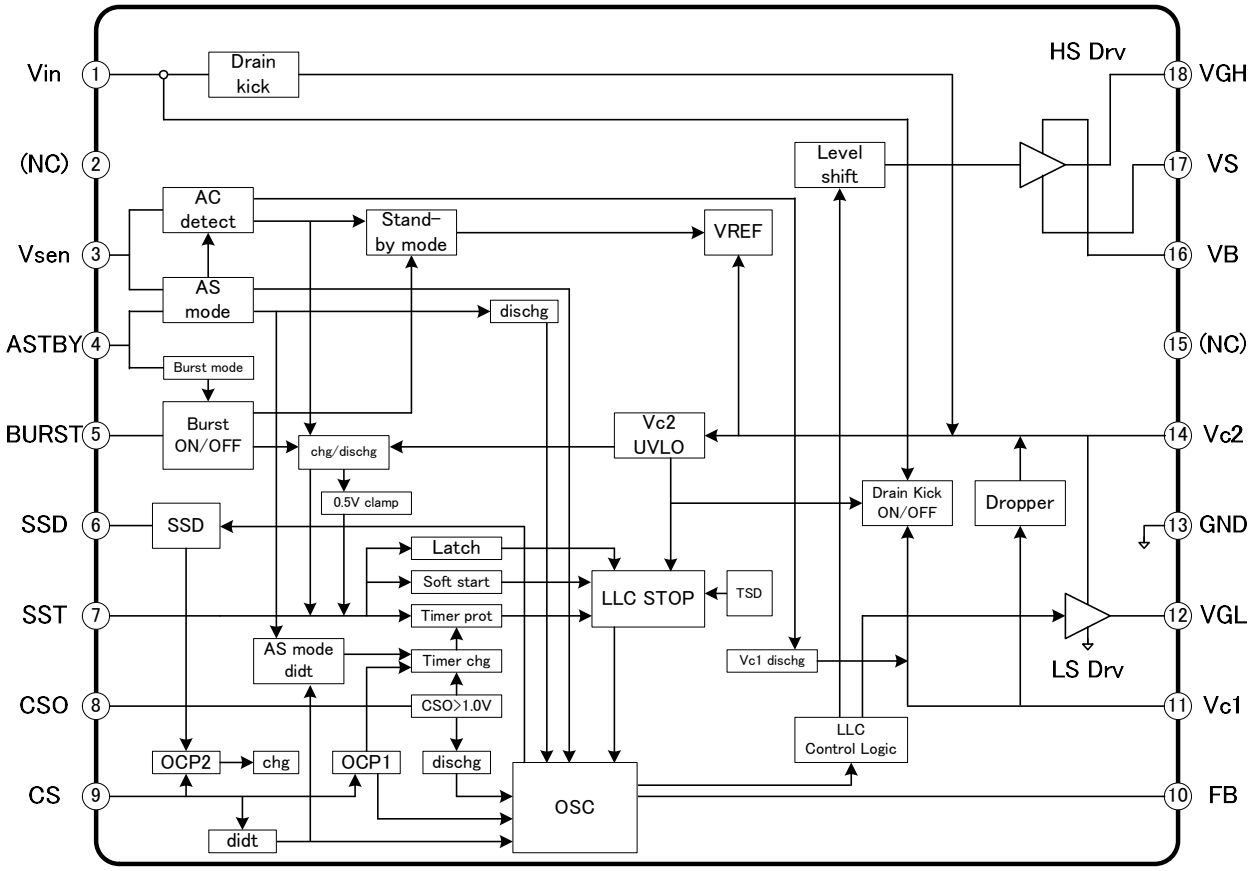


Figure 1 MCZ5211ST block diagram

1.3 Pin assignment diagram

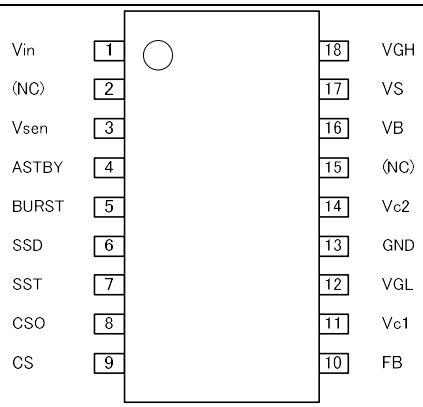


Figure 2 MCZ5211ST pin assignment diagram

1.4 Pin function list

Pin No.	Symbol	Function
1	Vin	**Startup circuit input pin** Input pin for the startup circuit
2	NC	**Pin not connected**
3	Vsen	**Low input protection, SS reset** Protects against low input voltage, turns remote on/off, resets SS.
4	ASTBY	**Active standby switching pin, burst mode switching pin** Switches to active standby mode and burst mode based on external signals.
5	BURST	**Burst operation control pin** Controls burst operation in burst mode.
6	SSD	**OCP2 threshold adjuster pin, normal/burst operating mode output pin** Sets operating mode output (normal/AS → 100 uA, burst → 0 uA) and OCP2 detection threshold.
7	SST	**Capacitor connector pin for soft start and abnormality detection intermittent operation** Determines the intermittent operation time for the LLC unit soft start time and OCP1/2 operation.
8	CSO	**Overcurrent averaging detection response adjustment pin** Pin for adjusting response for OCP 2 detection
9	CS	**Overcurrent detection, overcurrent averaging detection, di/dt (out-of-resonance) detection pin** Pin for LLC unit overcurrent (OCP1), overcurrent averaging (OCP2), and di/dt detection
10	FB	**Oscillator frequency setting pin: Duty and operating frequency control** Sets the output feedback, oscillation frequencies (fmin, fmax, fss), and dead time.
11	Vc1	**Control circuit power supply pin** Pin for control IC power supply
12	VGL	**Low-side driver output pin** Low-side gate drive pin
13	GND	**High-side driver reference power supply pin** Pin for IC ground connection
14	Vc2	**Driver power supply pin** Gate drive power supply pin
15	NC	**Pin not connected**
16	VB	**High-side driver power supply pin** High-side gate drive power supply pin
17	VS	**High-side driver reference power supply pin** Connected to the high-side MOS source and low-side MOS drain.
18	VGH	**High-side driver output pin** High-side gate drive pin

2 Basic Operations

*** Unless otherwise specified, MCZ5211ST threshold values are indicated by typical values in the characteristic specifications.**
For more information on the characteristic diagrams provided in this Application Note, refer to the characteristic diagrams in the characteristic specifications.

2.1 Operating modes

The MCZ5211ST has two control methods and three operating modes.

【Control methods】
a) Symmetric control
b) Asymmetric control

【Operating modes】
1) Normal mode
2) Active standby mode (AS mode)
3) Burst mode

The descriptions here assume normal mode unless otherwise specified.

Table 1 shows operation waveforms for symmetric control and asymmetric control.
Table 2 shows control and operation methods for each operating mode.

Table 1 Operation waveforms for symmetric control and asymmetric control

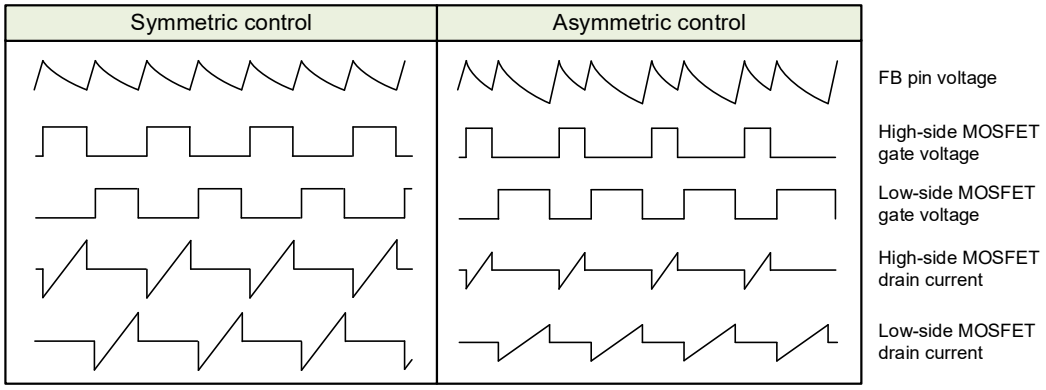


Table 2 Control and operation in each operating mode

Operating mode	Control method	Operation method
1) Normal mode	Symmetric control	Continuous operation
2) Active standby mode	Asymmetric control	
3) Burst mode		Burst operation

The operating sequences for the MCZ5211ST are described in Sections 2.2 and 2.3.
For more information on determining parameters for individual components, refer to Section 3.

2.2 Power supply section

The MCZ5211ST incorporates a startup circuit that does not require a startup resistance for ease of use with fewer components.

Figure 3 shows a schematic of the self-startup circuit.

The Vin pin charges capacitor C134 connected to the Vc2 pin from the high-voltage section when the power supply starts up; this consists of a high-withstand-voltage switch and constant current circuit.

After the power supply starts up, a voltage is generated in the auxiliary windings Nc. This is applied to the Vc1 pin via a diode. Note that the withstand voltage of the Vc1 pin is 35 V.

The voltage generated in Vc1 is supplied to Vc2 via an internal dropper in the IC.

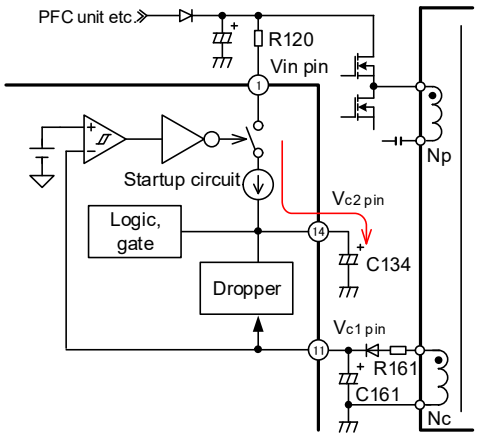


Figure 3 Schematic of the self-startup circuit

【R120 resistance】

In cases in which an abnormal short-circuit state can be foreseen, such as contact between the Vin pin and other low-voltage pins between the LLC unit input and the Vin pin, insert the R120 resistor as shown in Figure 3.

R120 should be designed so that sufficient drain kick supply current flows for the desired startup input voltage, and the voltage applied to the Vin pin does not fall below the minimum recommended operating condition of 50 V. R120 should ideally be a fuse resistance in the range 1 kΩ to 2.2 kΩ.

【R161 resistance】

Insert the limiting resistance R161 between the auxiliary windings Nc and Vc1 pin to regulate the short-circuit current at power supply startup. The resistance of R161 depends on the capacitance of C161, but it should normally be in the range 1.5 Ω to 47 Ω for a capacitor of between 100 uF and 220 uF.

Note that R161 will be subjected momentarily to the current charging C161 at power supply startup, so it is recommended that pulse/surge resistant resistors be used.

And while increasing the resistance of R161 will regulate the current, it will also slow the voltage rise in C161 at power supply startup and in burst mode, so the resistance of R161 should be adjusted by checking the startup time and burst operation.

Table 3 Power supply threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
Drain kick supply current 1	Idk(on)1	Vin=100V、Vc2=1.0V	2.8	mA
Drain kick supply current 2	Idk(on)2	Vin=100V、Vc2=4.0V	33	mA
Drain kick supply current 1/2 switching Vc2 voltage	Vc2(dkon12)	Idk=Idk(on)1→ Idk(on)2	2.5	V
Vc2 voltage with drain kick on	Vc2(dkon)	Vin=100V、Vc1=0V	12.8	V
Vc2 voltage with drain kick off	Vc2(dkoff)	Vc1=16V	12.5	V
Drain kick stop Vc1 voltage	Vc1(dkoff)	Vin=100V	12.6	V
Drain kick restart Vc1 voltage	Vc1(dkon)	Vin=100V	8.0	V
Vc2 operation start voltage	Vc2(st)		10	V
Vc2 operation stop voltage	Vc2(sp)		7.5	V

Figure 4 shows the operating sequence for power supply startup.

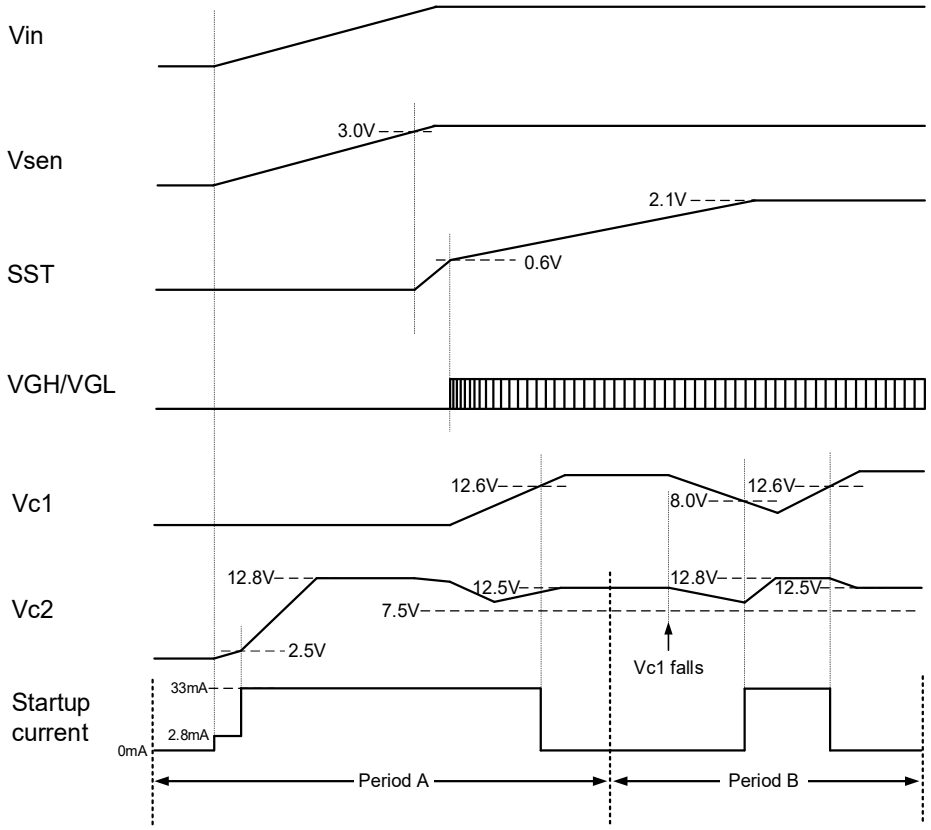


Figure 4 Startup sequence diagram

The supply current from the Vin pin to the capacitor C134 connected to the Vc2 pin varies due to the Vc2 pin voltage.
When Vc2 is 1 V, Idk(on)1 is 2.8 mA, and when Vc2 is 4 V, Idk(on)2 is 33.0 mA.

【Period A】

If the Vc1 pin voltage is less than the Vc1(dkoff) voltage of 12.6 V at power supply startup, the Vc2 pin voltage is charged until it reaches 12.8 V. If the Vc2 pin voltage is 10 V or more and the Vsen pin voltage is 3.0 V or more, the SST pin charging starts, and once the SST pin voltage reaches the Vss(st) voltage of 0.6 V, the LLC unit gate is output and the power supply operation starts.

When the power supply activates and a voltage is generated in the auxiliary windings Nc, the capacitor C161 is charged and the Vc1 pin voltage rises. Once the Vc1 pin voltage is at least the Vc1(dkoff) voltage of 12.6 V, the startup circuit is isolated and supply is provided by the auxiliary windings only. In this case, the Vc2 pin voltage is clamped at the Vc2(dkoff) voltage of 12.5 V.

【Period B】

If the Vc1 pin voltage drops to or below the Vc1(dkon) voltage of 8.0 V, the startup circuit will resume operation. Note that the MCZ5211ST will stop if the Vc2 pin voltage drops to the Vc2(sp) voltage of 7.5 V.

Insert the capacitors C134 and C161 connected to the Vc1 and Vc2 pins with sufficient capacitance to ensure stable operation in transient states such as startup and shutoff. The capacitance will depend on the desired input/output conditions but should ideally be around 100 uF to 470 uF.

Malfunctions may result due to noise input to the Vc1 and Vc2 pins if the C134 or C161 capacitors are beyond a certain distance from the MCZ5211ST Vc1 and Vc2 pins. In such cases, add an MLCC with capacitance of approximately 0.1 uF to 1.0 uF close to the Vc1 and Vc2 pins to prevent malfunctions.

2.3 Individual pin operation details

2.3.1 Gate driver output (VGL, VGH pins)

The gate output is output from the VGL (low-side MOSFET) and VGH (high-side MOSFET) pins. For more information on gate output timing, refer to Section 2.3.2.

The LLC gate driver drive capability is **0.24 A (source) and 0.40 A (sink)**. These values are designed to allow the MOSFET to be driven at sufficiently high speed without causing signal-related malfunctions.

Figure 5 (A) shows a typical drive circuit example.

If a MOSFET with a large Qg is used, connect a sink diode as shown in **Figures 5 (B) and (C)**. When using a sink diode, use a low capacitance Schottky diode. Do not use a snappy (hard) recovery diode. We recommend using a Shindengen **D1NS4** (axial) or **M1FM3** (surface mounted) diode.

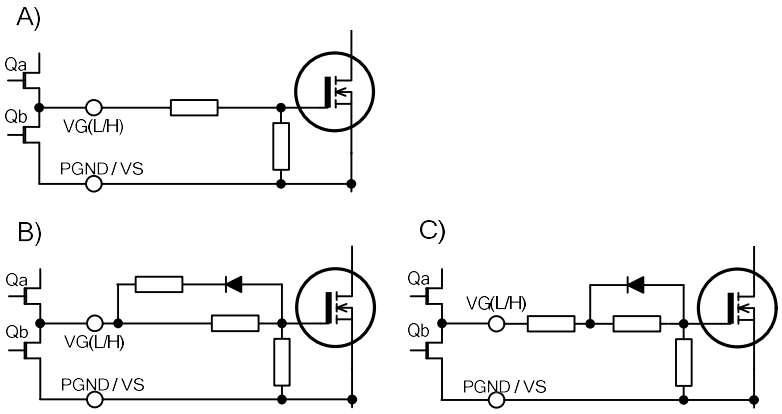


Figure 5 Gate drive circuit examples

Table 4 Drive capability threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
Source drive capability	Iout(so)	VGL=VGH=0V	-240	mA
Sink drive capability	Iout(si)	VGL=VGH=12V	400	mA

2.3.2 Oscillation control section (FB pin)

The MCZ5211ST oscillation frequency is determined by the charge and discharge of the capacitor Ct connected to the FB pin.

VGL and VGH output alternately while Ct discharges.

While Ct is charging, a dead time (DT) will result in which both the VGL and VGH outputs are off (see **Figure 6**).

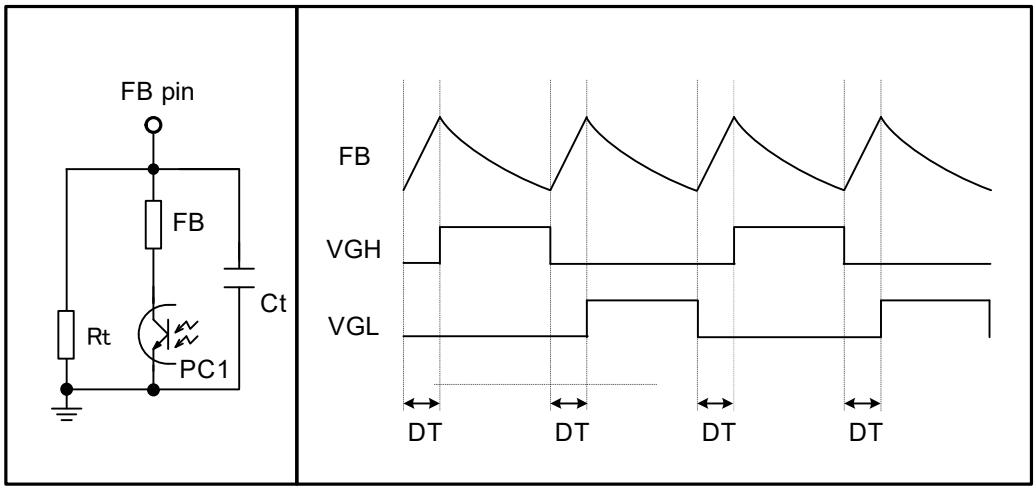
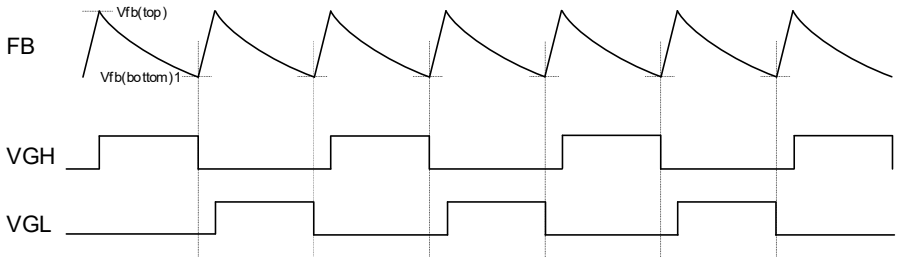
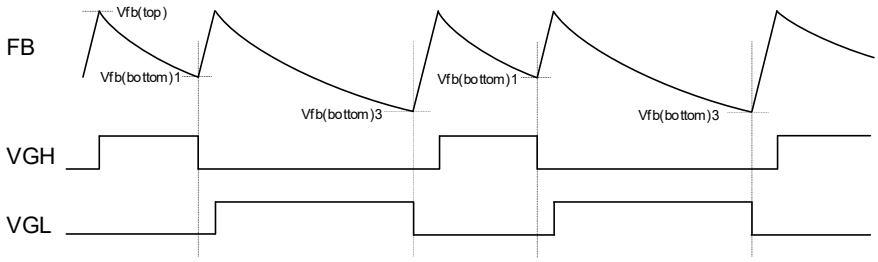


Figure 6 FB and VGL/VGH operation waveforms

Figure 7 shows the FB pin charge and discharge timing in each operating mode.



(A) Normal mode



(B) Active standby mode and burst mode

Figure 7 Gate on/off timing in each operating mode

The MCZ5211ST is a frequency and ON duty modulated IC. The oscillation frequency is controlled by the FB pin current (see **Figure 8**).

Dead time is widely controlled when the frequency is at the maximum, such as for light loads, making it easy to ensure ZVS (zero voltage switching) over the entire frequency range.

The minimum oscillation frequency (fmin) is determined by the external resistance Rt connected in parallel with the Ct capacitor connected to the FB pin.

The maximum oscillation frequency (fmax) is determined by the Rt and FB resistances connected in parallel with the Ct capacitor connected to the FB pin. It is recommended that the maximum oscillation frequency fmax does not exceed **500 kHz** during continuous operation. The initial oscillation frequency fss during soft startup also varies based on the Ct capacitance. (Refer to Section 2.3.6.)

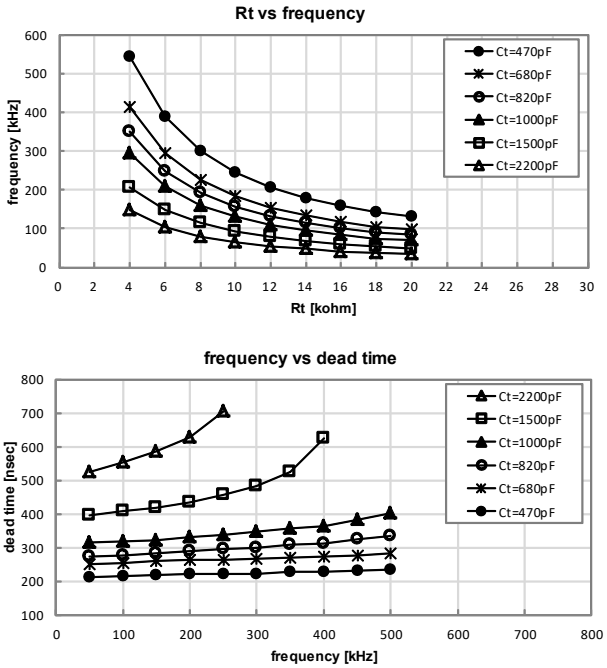


Figure 8 Correlation between Rt resistance and oscillation frequency (top) and between oscillation frequency and dead time (bottom)

Table 5 FB pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
FB charging current	Ifb(chg)	FB=4V	-9.0	mA
FB charge stop voltage	Vfb(top)		5.00	V
FB charge start voltage 1	Vfb(bottom)1		3.75	V
FB charge start voltage 3	Vfb(bottom)2	ASTBY=open	2.7	V

2.3.3 Brownout protection (Vsen pin)

The Vsen pin monitors the input voltage and prohibits gate drive output and controls the SST pin charging/discharging voltage in accordance with that value. This function prevents out-of-resonance operation due to the application of an input voltage while Vc1 is applied or momentary drop or cut-out of the input voltage. For more information on individual pin voltages and timing, refer to **Figure 9**.

The SST pin is charged once the Vsen pin voltage reaches the **Vsen1(ss-reset) voltage of 3.00 V** while the input voltage is rising. Gate output starts once the SST pin voltage reaches the **Vss(st) voltage of 0.6 V** or higher. This begins startup while the oscillation frequency is high immediately after oscillation starts, and ensures a safe startup by reducing the oscillation frequency as the SST pin is gradually charged. (For more information on the SST pin function, refer to **Section 2.3.6**.)

The SST pin is discharged once the Vsen pin voltage reaches the **Vsen2(ss-reset) voltage of 2.75 V** or lower while the input voltage is decreasing. As the SST pin is discharged, the oscillation frequency is gradually increased. The gate output is stopped once the SST pin voltage reaches the **Vss(sp) voltage of 0.5 V** or lower. This starts oscillation from a high oscillation frequency when the Vsen pin voltage reaches **Vsen1(ss-reset)** or higher again, preventing out-of-resonance operation.

Since the Vsen SS-Reset threshold value includes hysteresis, this prevents Vsen on/off malfunctions due to factors such as PFC output voltage ripple.

Note that the Vsen pin on/off threshold value is switched automatically depending on the individual mode, as shown in Table 6.

Table 6 Vsen on/off threshold values for each operating mode

Operating mode	Vsen ON (Vsen 1 or 3)	Vsen OFF (Vsen 2 or 4)
Normal mode	3.00V	2.75V
Active standby mode	0.85V	0.75V
Burst mode	0.85V	0.75V

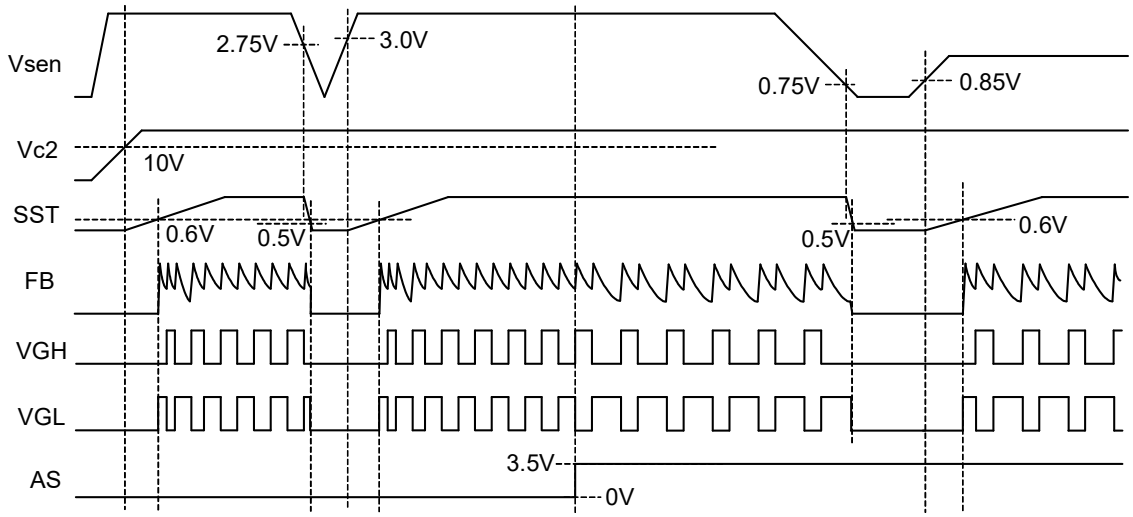


Figure 9 Vsen pin and individual output timing chart (for AS off and AS on operations)

Table 7 Vsen pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
Input voltage monitoring threshold 1	Vsen1	ASTBY<Vas(stpoff)	3.00	V
Input voltage monitoring threshold 2	Vsen2	ASTBY<Vas(stpoff)	2.75	V
Input voltage monitoring threshold 3	Vsen3	ASTBY>Vas(stpoff)	0.85	V
Input voltage monitoring threshold 4	Vsen4	ASTBY>Vas(stpoff)	0.75	V

2.3.4 Overcurrent protection function (CS/CSO pins)

The MCZ5211ST includes an overcurrent protection function, and this uses the CS pin for detection.

Figure 10 shows a CS and CSO pin connection example.

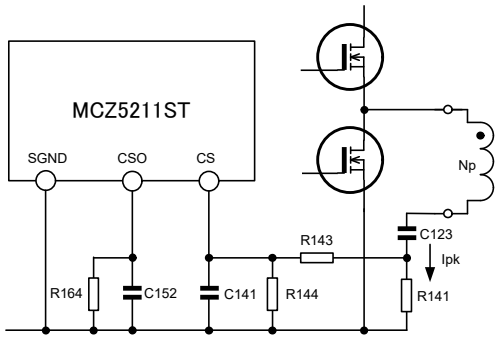


Figure 10 CS and CSO pin connection example

As shown in Figure 10, the current flowing through the resonant capacitor C123 is detected by the current detection resistance R141 and is connected to the CS pin divided by the dividing resistances R143 and R144. For more information on determining individual resistance values, refer to Section 3.4.

The CS pin has three threshold values for the positive, negative, and both directions, respectively, and three protection functions operate according to the voltage level. The protection functions here are defined as OCP1, OCP2, and di/dt, respectively.

Table 8 Three overcurrent protection functions

	Symbol	Name	CS pin threshold value condition
①	OCP1	Cycle by cycle OCP	CS pin voltage exceeds ±0.550 V
②	OCP2	Frequency limit OLP	CS pin voltage exceeds ±0.350 V
③	di/dt	Capacitive mode protection	CS pin voltage is below ±0.060 V

*OCP: Overcurrent protection, OLP: Overload protection

【OCP1】

OCP1 activates if the CS pin exceeds ±0.550 V.

Figure 11 shows an example in which OCP1 detection is triggered while the high-side MOSFET is on.

OCP1 detection is triggered if the CS pin voltage exceeds +0.550 V during the high-side period. Similarly, OCP1 detection is triggered if it falls below -0.550 V during the low-side period.

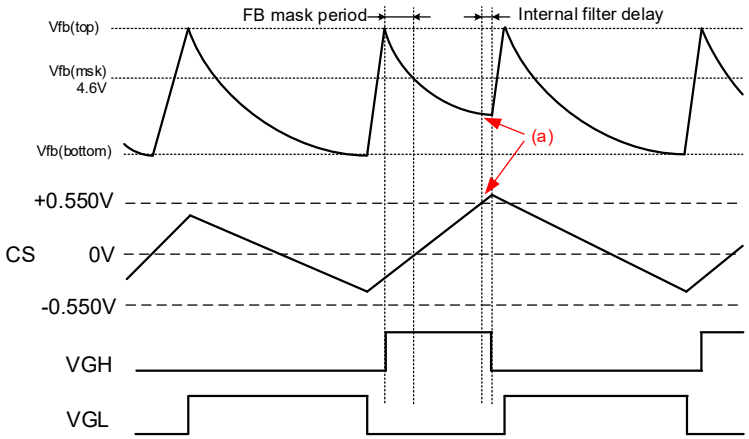


Figure 11 OCP1 operating sequence

The MCZ5211ST performs the following control operations when OCP1 detection is triggered:

(a) The FB pin is switched to the charging period, and the gate output (VGH or VGL) is turned off.

(b) The SST pin is charged at 40 uA for eight FB charge/discharge cycles.

(c) The CSO pin is charged at 25 uA for the period up to the FB mask voltage in the next cycle after OCP1 detection.

The gate output turns off immediately when OCP1 is detected, enabling the current peak flowing to the MOSFET to be regulated and preventing overcurrent and transformer saturation during abnormal situations. Additionally, charging the SST pin enables the latch to be stopped after intermittent timer operation in case of a prolonged abnormal situation, preventing overheating of the MOSFET and other components.

Note that if OCP1 is not detected again within eight FB charge/discharge cycles after OCP1 has been detected, the SST pin discharges at the timer discharging current (refresh) of 600 uA until it reaches 2.1 V.

((FB mask period))

The CS pin is masked to prevent an OCP1 detection malfunction due to noise generated by switching when the MOSFET turns on and off. This prevents OCP1 from operating from the start of FB pin discharge until it falls to or below the FB mask voltage. Thus, the OCP1 operation is not performed even if the threshold is exceeded during this period. If fmin is designed too low, the OCP1 threshold value may be exceeded and masked while the FB mask voltage is exceeded. Therefore, use an appropriate fmin value in the design.

((Internal filter))

An approximately 200 ns internal filter is included to prevent malfunctions due to noise generated by external factors. This results in a delay of approximately 200 ns from when the CS pin exceeds the OCP1 threshold until FB is charged.

((When OCP1 and OCP2 are detected simultaneously))

The OCP1 detection voltage is set to a higher value than the OCP2 detection voltage. This means OCP2 will also exceed the detection voltage while OCP1 is operating; if both OCP1 and OCP2 are simultaneously detected, this sequence ensures that OCP1 detection takes precedence.

【OCP2】

OCP2 activates if the CS pin exceeds ±0.350 V.
The MCZ5211ST performs the following control operations when OCP2 activates:

(a) The SST pin is charged for eight FB charge/discharge cycles. The charging current varies based on the CSO pin voltage.

- 0.9 V ≤ CSO < 1.0 V: The SST pin is not charged.
- 1.0 V ≤ CSO < 2.0 V: The SST pin is charged at 1.7 uA.
- 2.0 V ≤ CSO ≤ 2.5 V: The SST pin is charged at 40 uA.

(b) The CSO pin is charged at 30 uA for the period up to the FB mask voltage in the next cycle after OCP2 detection.

As with OCP1, OCP2 includes an FB mask period and internal filter. If fmin is designed too low, the OCP2 threshold value may be exceeded and masked while the FB mask voltage is exceeded. Therefore, use an appropriate fmin value in the design.

Note that if OCP2 is not detected again within eight FB cycles after OCP2 has been detected, the SST pin discharges at the timer discharging current (refresh) of 650 uA until it reaches 2.1 V.

【CSO】

The CSO pin controls the oscillation frequency based on the CSO pin voltage. Figure 12 shows the relationship between the CSO pin voltage and the oscillation frequency. The CSO pin is pre-charged inside the IC and is normally maintained at 0.9 V.

When OCP1 and OCP2 activate, the CSO pin is charged as shown in Figure 13. When the CSO pin voltage reaches 1.0 V or higher, the oscillation frequency increases based on the CSO pin voltage. The output power is limited by increasing the oscillation frequency. Note that the CSO pin is charged up to a maximum voltage of 2.5 V.

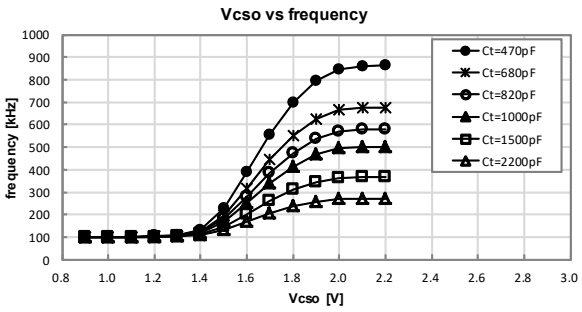


Figure 12 CSO voltage against oscillation frequency

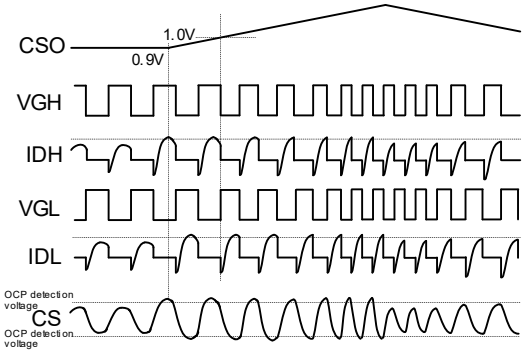


Figure 13 CSO voltage operating sequence

【di/dt】

As shown in Figure 14, di/dt activates when the CS pin detects a negative edge below ±0.060 V.

The MCZ5211ST performs the following control operations when di/dt activates:

(a) The FB pin is switched to the charging period, and the gate output (VGH or VGL) is turned off.

(b) The SST pin is charged depending on the operating mode.
- Normal mode: The SST pin is not charged.
- Active standby mode: The SST pin is charged at 40 uA for eight FB charge/discharge cycles.
- Burst mode: The SST pin is charged at 40 uA for eight FB charge/discharge cycles.

The gate output is turned off immediately when di/dt activates, enabling prevention of out-of-resonance operation (capacitive mode) to prevent MOSFET overheating and damage.

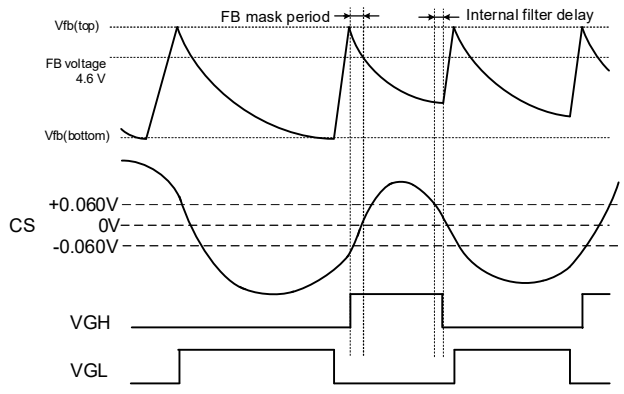


Figure 14 di/dt operating sequence

As with OCP1 and OCP2, di/dt includes an FB mask period and internal filter.
If fmin is designed too low, the di/dt threshold value may be detected and masked while the FB mask voltage is exceeded. Therefore, use an appropriate fmin value in the design.

Table 9 shows the correlation between the timer and CSO charging for each detection mode.

Table 9 Correlation between the timer and CSO charging operations for each detection mode

Detection mode	Operating mode	Timer charging	CSO charging
OCP1 detection	Normal mode	(A)	(B)
	Active standby mode		
	Burst mode		
OCP2 detection	Normal mode	(C)	(D)
	Active standby mode		
	Burst mode		
di/dt detection	Normal mode	None	None
	Active standby mode	(A)	
	Burst mode		

(A) The SST pin is charged at 40 uA for eight FBL cycles.

(B) The CSO pin is charged at 25 uA for the period up to the FB mask voltage in the next cycle after OCP1 detection.

(C) The SST pin is charged at 1.7 uA (1 V ≤ Vcso < 2.0 V) or 40 uA (2.0 V ≤ Vcso) for eight FBL cycles.

(D) The CSO pin is charged at 25 uA for the period up to the FB mask voltage in the next cycle after OCP2 detection.

Table 10 CS/CSO pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
OCP1(+) detection voltage	Vocp1(+)		0.550	V
OCP1(-) detection voltage	Vocp1(-)		-0.550	V
OCP2(+) detection voltage 1	Vocp2(+)1	SSD=4V	0.350	V
OCP2(-) detection voltage	Vocp2(-)		-0.350	V
di/dt(+) detection voltage	Vdidt(+)		0.060	V
di/dt(-) detection voltage	Vdidt(-)		-0.060	V
CSO pin pre-charge voltage	Vcso(pre)	CS=0V	-100	uA
OCP2 operation start CSO pin voltage	Vcso(ocp2)		1.0	V
Timer charge switching CSO pin detection voltage	Vcso(tmr)		2.0	V
CSO pin charging current during OCP2 operation	Icso(ocp2)	CSO>Vcso(ocp2)	-25	uA
CSO pin discharging current	Icso(dis)	CSO=1.2V	10	uA

2.3.5 OCP2 input voltage correction (CS/SSD pins)

The MCZ5211ST features a built-in circuit to correct the overcurrent protection operating point when the input voltage fluctuates.
Input voltage corrections are performed by varying the OCP2 detection threshold value. The OCP2 detection threshold value varies based on the SSD pin voltage and FB pin voltage.

Figure 15 is a schematic diagram showing the drooping characteristics with and without the input correction function.
Corrections are performed to facilitate OCP2 detection, particularly when a high input voltage is applied. This correction level can be adjusted by adjusting the value of the resistance connected to the SSD pin.

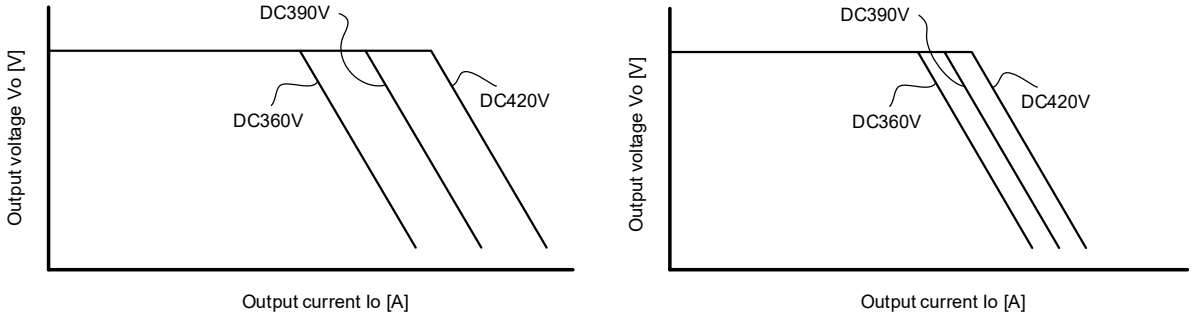


Figure 15 Drooping characteristics schematic diagrams without OCP2 input correction function (left) and with correction function (right)

Figure 16 shows the resonance curves and operation waveforms for the LLC current resonance circuit.
As shown by the operation waveforms in Figure 16 (a), the oscillation frequency during operation changes based on the input voltage. Typically, a lower input voltage increases the peak of the current waveform for the same load. The resonance frequency fr remains constant regardless of the input voltage.

Assuming that the overcurrent protection function activates at the point at which the MOSFET current value reaches its peak (points X and Y) as shown in Figure 16 (b), where it reaches the peak while the gate is on changes based on the input voltage. In the example shown in Figure 16 (b), if the period while the gate is on is 1, the current peak will come during the on-period with a duty ratio of 0.8:0.2 when the input voltage is high. Conversely, if the input voltage is low, the current peak will come during the on-period with a duty ratio of 0.4:0.6.

If the gate is on when the input voltage is low, the current peak will come before the on-period (point Y). If the input voltage is high, it will come later in the on-period (point X). The OCP2 input voltage is corrected using this resonance characteristic.

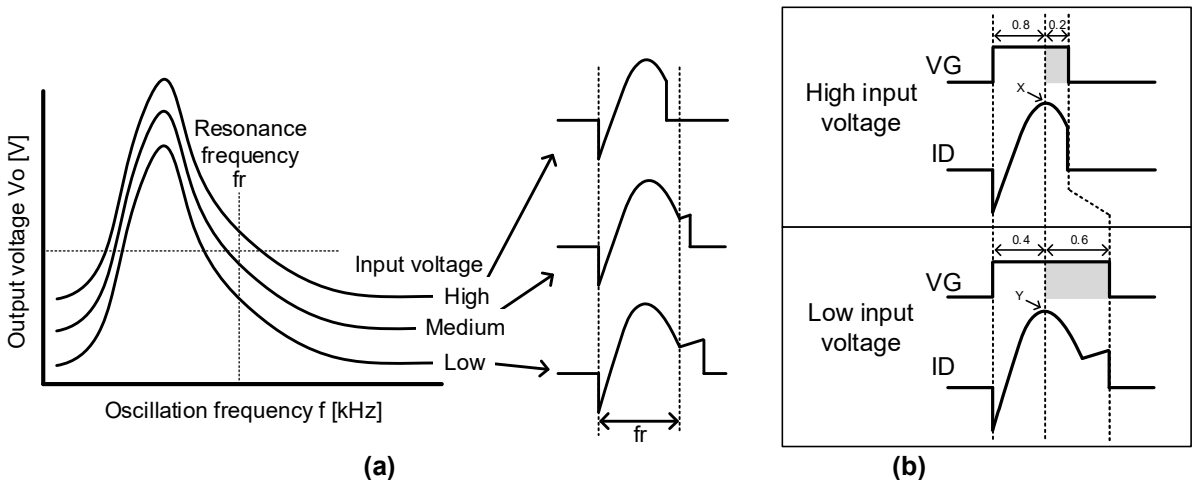


Figure 16 (a) Input voltage and operation waveforms, (b) Correlation between input voltage and current peak

Input corrections are adjusted by varying the OCP2 detection threshold so that OCP2 can be detected easily. The input correction level is determined by the SSD pin. Figure 17 shows the SSD pin peripheral circuit diagram. Figure 18 shows the relationship between the SSD voltage and the value of the external resistance connected to the SSD. The SSD pin is charged from within the IC using a current of -100 uA. Thus, the SSD pin voltage is determined by the value of the external resistance.

As shown in Table 11, the SSD pin charging current switches in normal/AS mode and burst mode.

Table 11 Correlation between SSD charging current and operating mode

ASTBY pin voltage	Operating mode	SSD charging current	CS input correction
0V ≦ ASTBY ＜ 2.2V	Normal mode	-100uA	Yes
2.2V ≦ ASTBY ＜ 3.0V	Asymmetric step mode		
3.2V ≦ ASTBY ＜ 4.0/3.9V	Active standby mode		
4.0/3.9V ≦ ASTBY ≦ 5.2V	Burst mode	-0uA	No

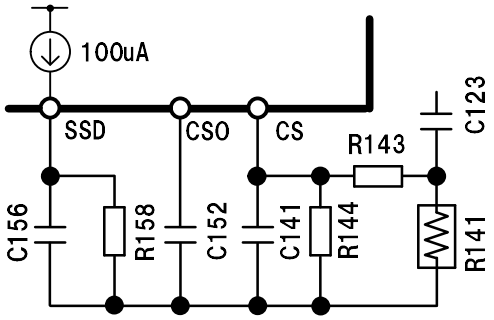


Figure 17 SSD pin connection diagram

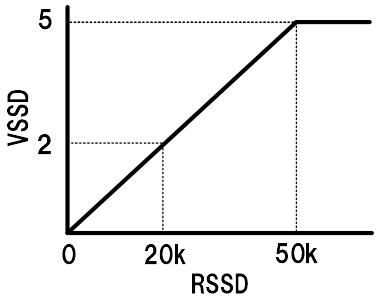


Figure 18 Correlation between SSD resistance and SSD voltage

Figure 19 (b) and (c) show the relationship between the SSD pin voltage and the OCP2 threshold. Vocp2(+)1 is the OCP2 detection threshold operation start voltage and is constant at 0.35 V. Vocp2(+)2 is the OCP2 detection threshold lower limit voltage and is set by the SSD pin voltage. As shown in Figure 19 (a), the OCP2 detection threshold is fixed at Vocp2(+)1 as far as the FB mask voltage Vfb(msk) and is gradually reduced based on the FB pin voltage when it is below Vfb(msk). The OCP2 detection threshold will be Vocp2(+)1 at the point at which the FB pin voltage reaches the FB charge start voltage 1 Vfb(bottom1). Note that an input correction circuit is included only during the high-side period. During the low-side period, the threshold value remains at -0.35 V regardless of the FB pin voltage.

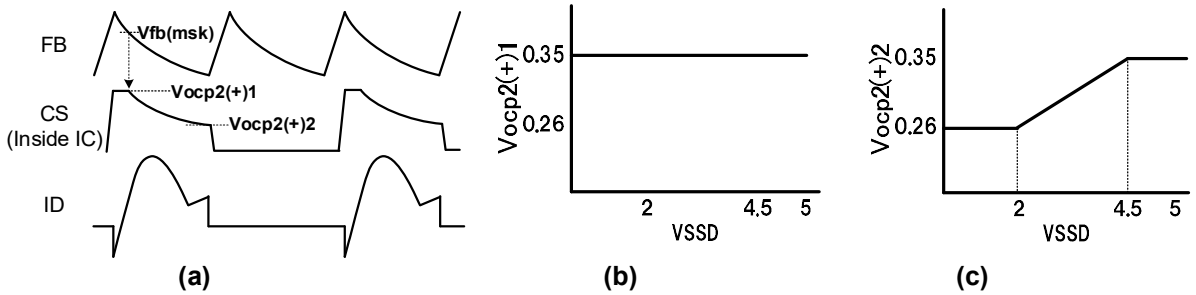


Figure 19 (a) CS threshold waveforms, (b) Vocp2(+)1 threshold value, (c) Vocp2(+)2 threshold value

Table 12 SSD pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
SSD pin charging current 1	Issd(chg)1	ASTBY<Vastby(bston/off)	-100	uA
SSD pin charging current 2	Issd(chg)2	ASTBY>Vastby(bston/off)	0	uA
SSD pin open voltage	Vssd(open)		6	V
OCP2(+) detection voltage 2	Vocp2(+)2	SSD=1V	0.26	V

2.3.6 Soft start, di/dt protection at startup, latch stop function (SST pin)

(1) Soft start function

The LLC unit has a built-in soft start function, which gradually increases the oscillation frequency by charging the capacitor connected between the SST and GND pins. The following two conditions must be satisfied to charge the SST pin:

① The Vc2 pin voltage is at least the **Vc2(st) voltage of 10.0 V**.
② The Vsen pin voltage is at least **Vsen1(ss-reset) or Vsen3(ss-reset)**.

Oscillation starts when the SST pin voltage is at least 0.6 V and becomes constant at the **Vss(open) voltage of 2.1 V**. It also has hysteresis and stops oscillation at an SST pin voltage of 0.5 V or less. See **Figure 20** for the relationship between SST pin voltage and oscillation frequency.

The SS charging current for the SST pin has two levels depending on the SST pin voltage. Charging is at 90 uA when the SST pin voltage is between 0 V and 0.6 V, and at 30 uA when the SST pin voltage is 0.6 V or higher. This switches to accelerate charging to the LLC operation start SST voltage.

The SST pin is charged to 2.1 V and clamped at that voltage during normal operation.

The SST pin also has a timer intermittent latch stop function to reduce the load on the main switch and peripheral circuits during abnormal situations. For more information on the timer intermittent latch stop function, refer to **Section 2.3.6 (3)**.

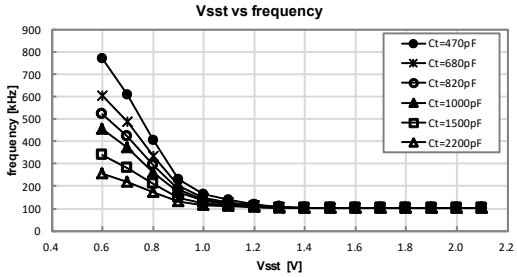


Figure 20 SST voltage and oscillation frequency

(2) di/dt protection at startup

Immediately after the LLC current resonance circuit power supply starts, the gate may turn off while the current flowing through the MOSFET flows through the body diode in the transient state in which the resonant capacitor voltage is unstable. In this state, a short-circuit current flows when the opposite MOSFET turns on due to the trr component of the body diode, and a load is applied to the MOSFET.

The MCZ5211ST includes a **Tss(3)** function to prevent the gate from turning off while the body diode is conducting at startup. As shown in **Figure 21**, the Tss(3) sequence extends the low-side VGL output by approximately 1.7-fold for the second time after the power supply starts. This enables the MOSFET to turn off the gate output after the current flows in the positive direction.

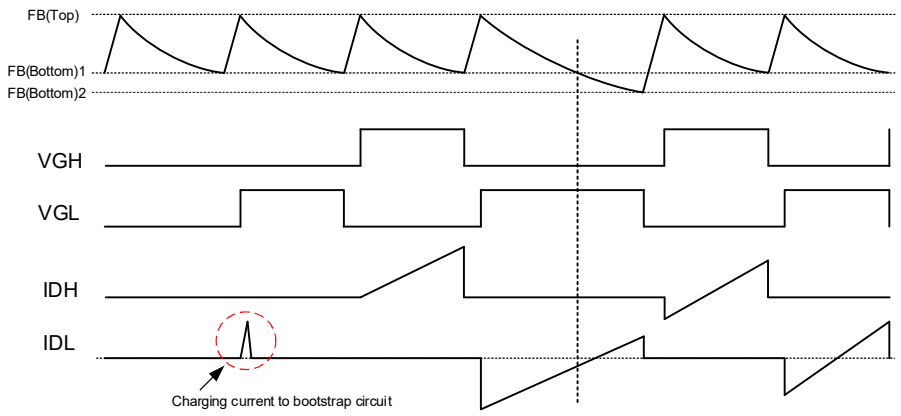


Figure 21 Tss(3) operating sequence

(3) Timer intermittent latch stop function during overcurrent protection function operation

The MCZ5211ST includes a function to stop latching after the intermittent timer activates during OCP1, OCP2 and di/dt operation. For more information on the timing and conditions for timer charging, refer to Table 9. For more information on the timer intermittent latch stop sequence, refer to Figure 22.

When an abnormal condition is detected, the SST pin is charged as shown in Figure 22. The timer charging current for charging the SST pin varies depending on the operating mode. Refer to Table 9 for the particular timer charging current value.

The SST pin includes a timer intermittent latch stop function. Csst will start charging beyond 2.1 V if either of the following two conditions ① or ② is met:

① OCP1 and OCP2 are operating.
② di/dt protection is operating in active standby mode.

If either of the above conditions continues and the SST pin voltage reaches the **Vtimer(set) voltage of 3.5 V** due to the continuous abnormal signal input, the mode will be intermittent operating mode. If the abnormal signal disappears during intermittent operating mode and if this intermittent oscillation mode is counted twice consecutively, the IC performs a latch-stop.

If latching is stopped, latching is released when the Vc2 pin voltage is equal or less than the latch release voltage of 7.0 V.

A latch counter reset function is also included, as shown in **Figure 22**. The two latch counter reset conditions are as follows:

① When SST = 2.1 V is reached (returning to normal operating mode without detecting OCP)
② SST refreshed (Vc2 on/off)

This function sets the latch counter to zero when the power supply functions normally. If the abnormal state persists, the latch counter is not reset, and the timer latch stops after counting twice.

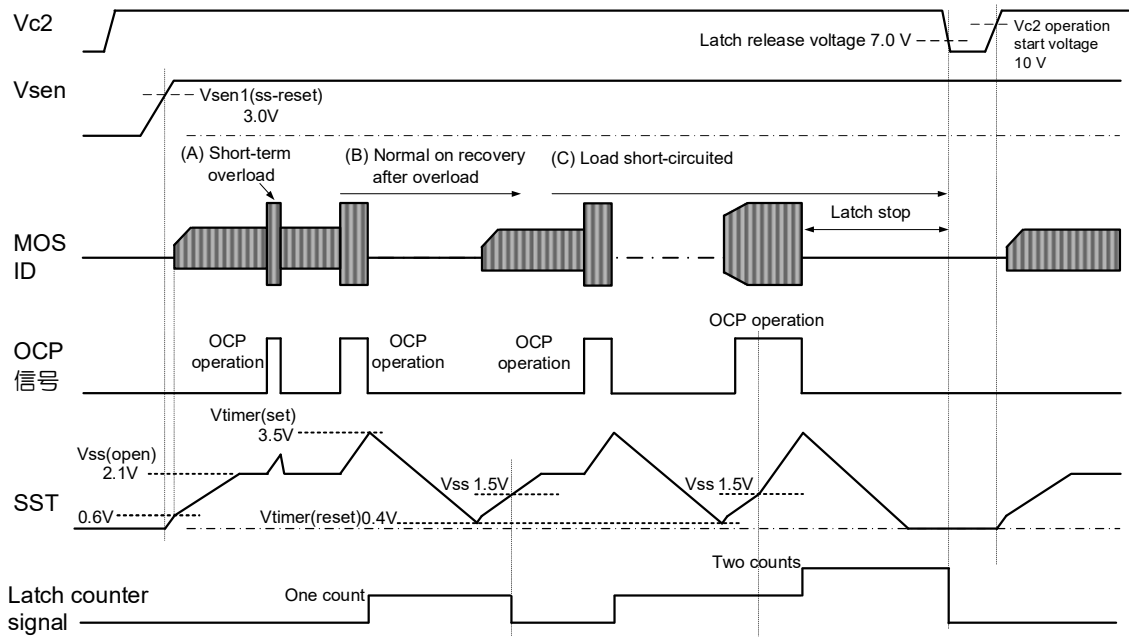


Figure 22 SST operating sequence

(4) Latch stop function

The MCZ5211ST incorporates a latch stop function to stop latching under abnormal conditions such as overvoltage on the secondary side. Figure 23 shows an example of the secondary side OVP circuit configuration.

The latch stop function is enabled by lifting the SST pin to 4.5 V from outside. Oscillation stops when the latch stop function is enabled.

To release the latch stop, the Vc2 pin voltage must not exceed the latch release voltage of 7.0 V. LLC unit oscillation starts when latching is released and the voltage exceeds the Vc2 operation start voltage once again.

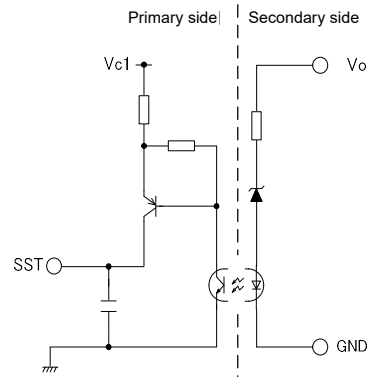
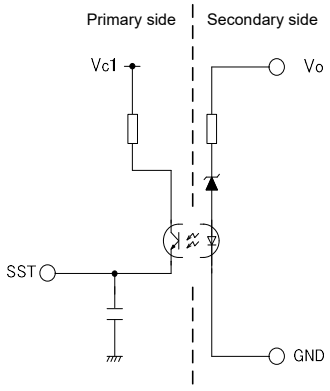
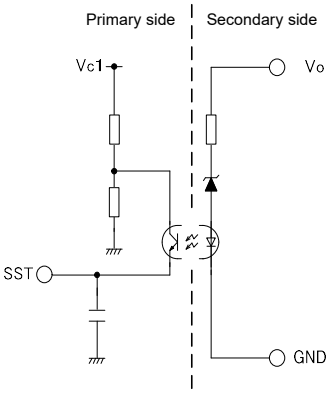
Example configuration ①	Example configuration ②	Example configuration ③
		
The fastest OVP operation of the three	Requires a photocoupler with high CTR if OVP operation is required for durations on the scale of several hundred usecs.	This configuration is used when OVP operation is possible for durations on the scale of several msecs.

Figure 23 Latch stop function circuit configuration examples

Table 13 SST pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
SST pin threshold value	Vsst		1.5	V
SST charging current 1	Isst(chg)1	SST=0V	-90	uA
SST charging current 2	Isst(chg)2	SST=1.0V	-30	uA
SST discharging current	Isst(dischg)	SST=1.0V、Vsen=0V	4.0	mA
SST pin open voltage	Vsst(open)		2.1	V
LLC operation start SST voltage	Vsst(st)		0.6	V
LLC operation stop SST voltage	Vsst(sp)		0.5	V
SST latch stop voltage	Vsst(latch)		4.5	V
Timer threshold value 1	Vtimer(set)		3.5	V
Timer threshold value 2	Vtimer(reset)		0.40	V
Timer charging current 1	Itimer(chg)1		-40	uA
Timer charging current 2	Itimer(chg)2		-1.7	uA
Timer charging current 3	Itimer(chg)3		-40	uA
Latch release voltage	Vc2(latch reset)		7.0	V
FB charge start voltage 2	Vfb(bottom)2	Tss(3)	3.10	V

2.3.7 High-side driver power supply (VB pin)

As shown in **Figure 24**, the floating power supply (VB) for the high-side MOSFET drive is generated by the bootstrap circuit, which uses the Dboot diode and Cboot floating smoothing capacitor towards the high-voltage side, using the Vc2 pin 12.5 V regulator output capacitor as the voltage source.

The potential difference between the low-side and high-side is maintained at the minimum using the bootstrap circuit due to the external Dboot, enabling a stable drive power supply even in the event of transients.

Cboot uses an MLCC. The recommended value is between **0.1 uF and 1.0 uF**. Dboot should use a diode with a withstand voltage of at least 600 V and high speed and soft recovery characteristics. We recommend the Shindengen **D1NK60** or **D1FK60** (for a PFC output voltage of approximately 400 V).

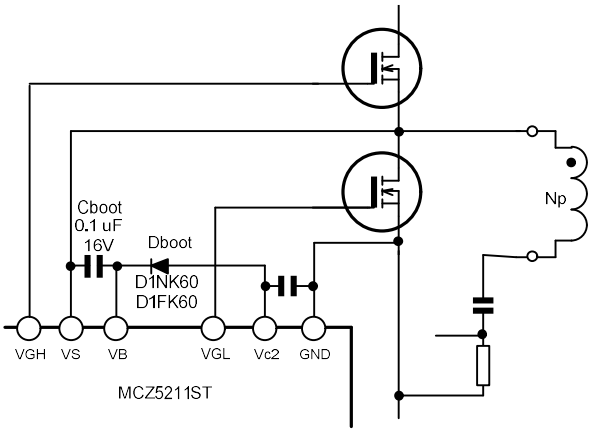


Figure 24 Bootstrap high-side Vcc generating circuit

Table 14 VB pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
High-side driver operation start voltage	VB-VS(st)		7.5	V
High-side driver operation stop voltage	VB-VS(sp)		5.5	V

2.3.8 Light load region loss improvement function (ASTBY/Burst pins)

Active standby mode and burst mode are controlled by ASTBY pin voltage.
For more information on the correlation between the ASTBY pin voltage and operating mode, refer to Table 15.

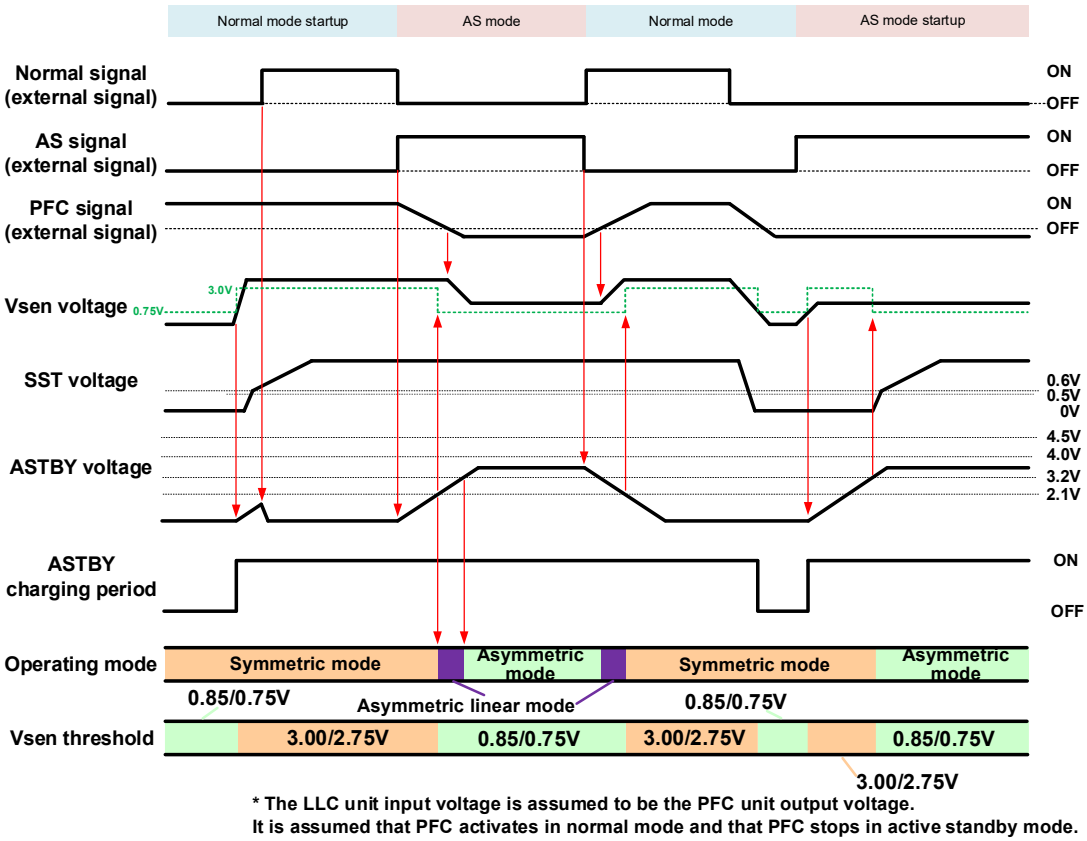
Table 15 ASTBY pin voltage and operating mode

ASTBY pin voltage	Operating mode	LLC unit
0V ≦ ASTBY ＜ 2.2V	Normal mode	Symmetric operation
2.2V ≦ ASTBY ＜ 3.0V	Asymmetric linear mode	Asymmetric operation
3.2V ≦ ASTBY ＜ 3.9V	Active standby mode	Asymmetric operation
4.0V ≦ ASTBY ≦ 5.2V	Burst mode	Asymmetric operation

* Demonstrates hysteresis from active standby mode to burst mode.
Switches from Active standby mode to Burst mode at ASTBY pin voltage 4.0 V.
Switches from Burst mode to Active standby mode at ASTBY pin voltage 3.9 V.

2.3.8.1 Active standby function

The active standby function enables lower losses in light load regions with a load of approximately 5 to 20 % of the rated load.
In active standby mode, asymmetric operation is performed with a high-side and low-side on width ratio of approximately 1:2. Figure 25 gives the detailed operating sequences for each threshold.



* The LLC unit input voltage is assumed to be the PFC unit output voltage.
It is assumed that PFC activates in normal mode and that PFC stops in active standby mode.

Figure 25 Active standby mode sequence

The on width ratio of the high-side and low-side MOSFET varies based on the ASTBY pin voltage.
When the ASTBY pin voltage is **0 V**, operation is symmetrical with an on width ratio of 1:1. When the ASTBY pin voltage is the **Vas(linoff) voltage of 2.2 V** or higher, the FB charge start voltage **Vfb(bottom)** for the low-side MOSFET decreases as shown in Figure 26, and the on width of the low-side MOSFET increases, resulting in asymmetric operation.

The FB charge start voltage **Vfb(bottom)** varies linearly according to the ASTBY pin voltage, and ASTBY pin voltage reaches the maximum on width ratio at the **Vas(linon) voltage of 3.0 V**. The on width ratio for the high-side and low-side MOSFETs at the maximum on width will be approximately 1:2.

If the ASTBY pin voltage is less than 2.2 V while in active standby mode, active standby mode is canceled, and the mode switches to normal mode.

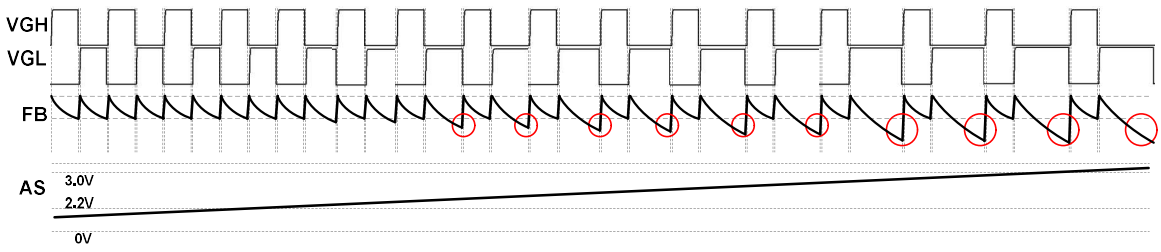


Figure 26 Gate waveform for AS linear operation

The MCZ5211ST incorporates a function to control the FB pin discharging current according to the ASTBY voltage and Vsen voltage to suppress overshooting (or undershooting) when switching between normal and active standby modes.

Figure 27 is a schematic diagram showing the correlation between the Vsen pin voltage and FB discharging current. Figure 28 shows the FB discharging current sequence when the ASTBY voltage varies.

As shown in Figure 27, the FB discharging current varies based on the Vsen pin voltage, and is 0 uA when Vsen is 3 V, and 400 uA when Vsen is 5 V. Further, as shown in Figure 28, the FB discharging current varies based on the ASTBY voltage while the ASTBY voltage is between 2.2 V and 3.0 V.

When the ASTBY voltage is less than 2.2 V, the FB discharging current will be 0 uA regardless of the Vsen voltage. When the ASTBY voltage is 3.0 V or higher, the FB discharging current is constant, with the value varying depending on the Vsen voltage.

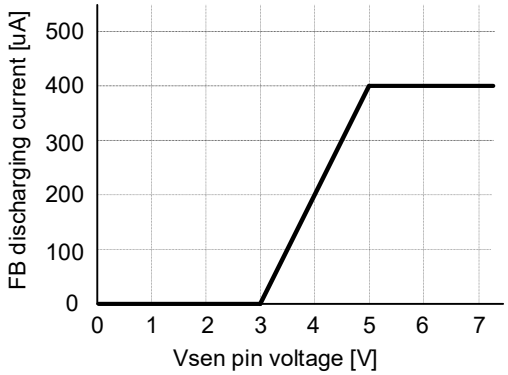


Figure 27 Correlation between Vsen voltage and FB discharging current (schematic diagram)

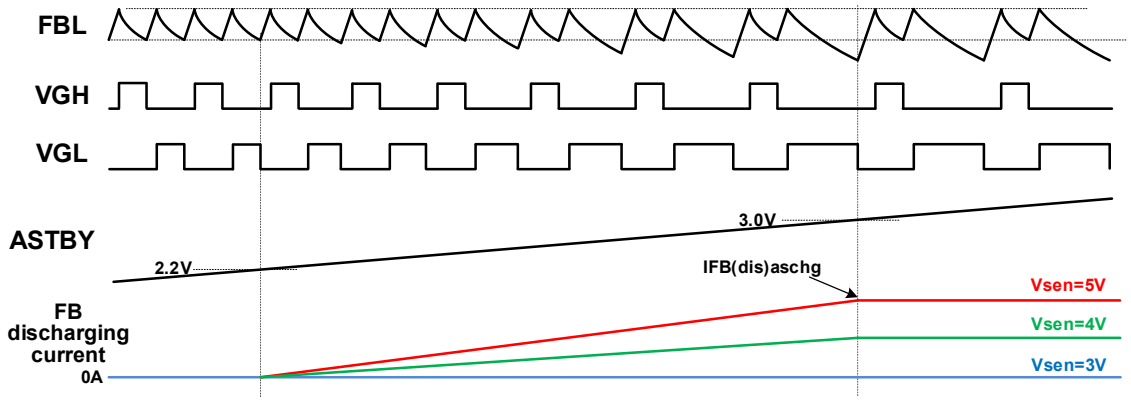


Figure 28 Operating sequence for ASTBY switching

2.3.8.2 Burst function

The burst function improves standby power during standby load. Burst mode is switched by the ASTBY pin. Oscillation start/stop is controlled by the burst pin.

Figure 29 shows examples of circuit configuration when using burst mode. Figure 29 (a) shows a configuration with two photocouplers in which the standby on/off section and burst mode output voltage lower limit detection section can be controlled independently. Figure 29 (b) shows a configuration with one photocoupler, allowing one photocoupler to be eliminated.

Burst mode is selected when the ASTBY pin is 4.0 V or higher. To cancel burst mode, set the ASTBY pin to 3.9 V or less. In normal mode and active standby mode, the burst pin is discharged with the burst pin discharging current of 400 uA. In burst mode, the burst pin discharging stops.

Once in burst mode, the burst pin is lifted by the transformer auxiliary winding voltage Vcc or a voltage split from an external circuit, and when the burst pin output stop voltage is at least 2.0 V, the SST pin is discharged and the LLC unit oscillation stops. Next, when the burst pin output start voltage drops to 1.5 V or less, SST pin charging starts and the LLC unit oscillation starts. See Figure 31 for the detailed sequence. Figure 32 shows the operating sequence for active standby and burst modes.

In burst mode, the SST charging current at soft start is the Isst(chg)3 current of -90 uA. This reduces the soft-start time, enabling the oscillation time to be shortened during burst operation, and also helps to improve standby power.

Note that in normal mode and active standby mode, the SSD pin is charged with the SSD pin charging current 1 (Issd(chg)1) of -100 uA. Once in burst mode, SSD pin charging stops. This means that in the configuration shown in Figure 30, in normal and active standby modes, the capacitance will be determined by C154; in burst mode, the capacitance will be determined by C153 and C154 in series.

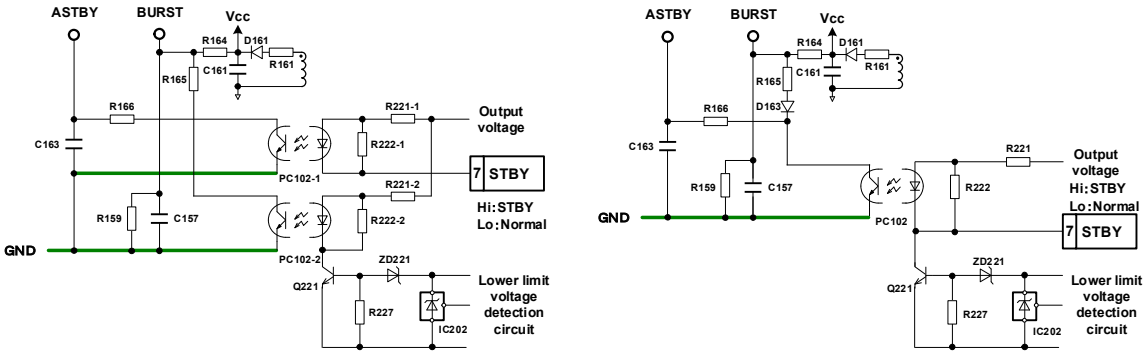


Figure 29 Burst pin connection examples
(a) With two photocouplers, (b) With one photocoupler

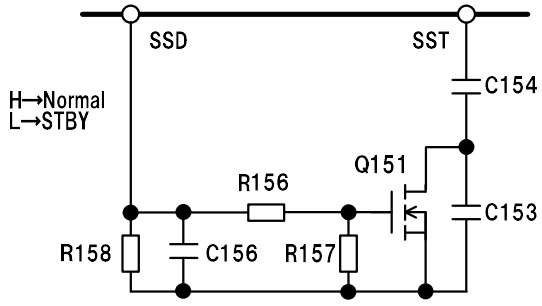


Figure 30 Burst switching configuration example

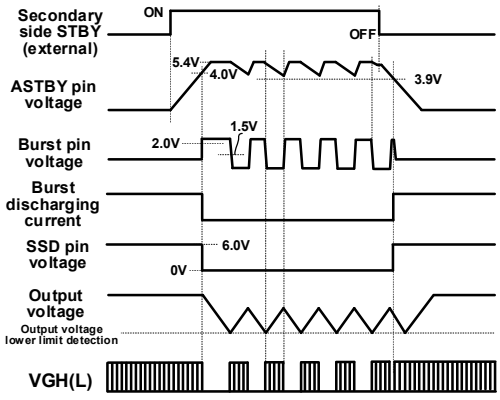
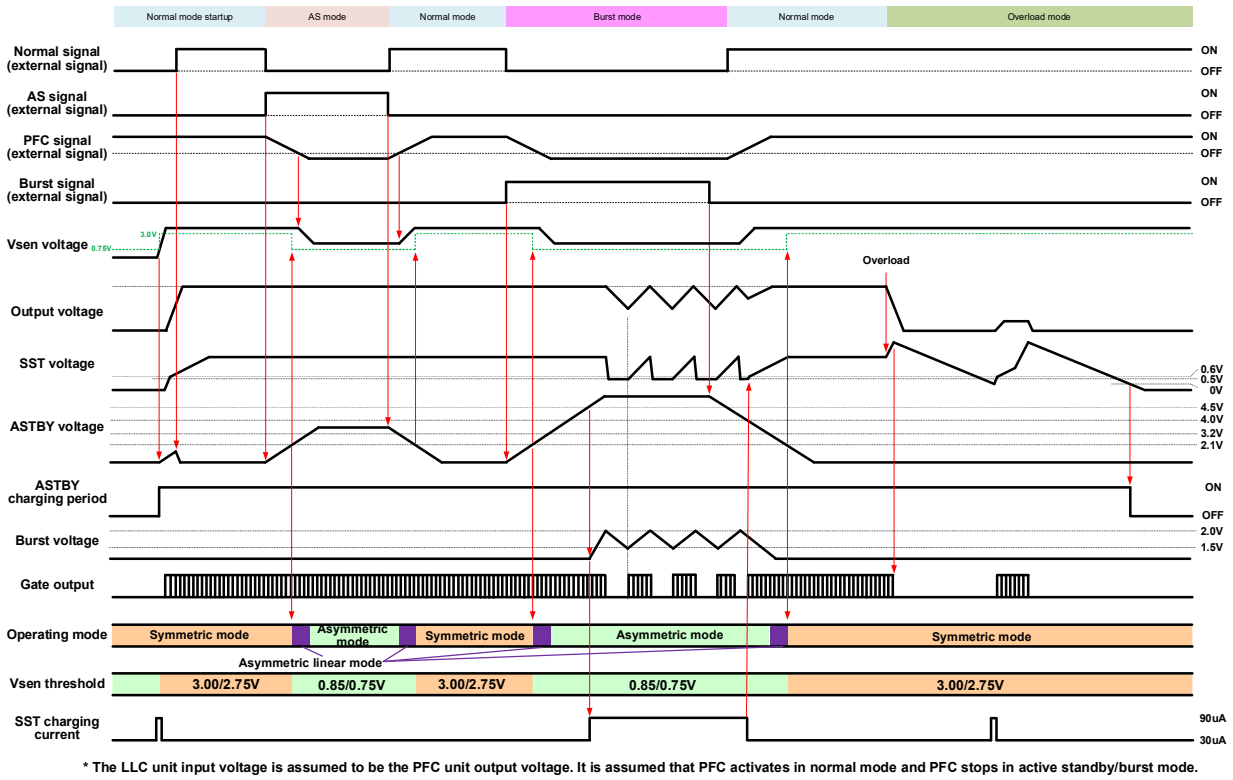


Figure 31 Burst operating sequence



* The LLC unit input voltage is assumed to be the PFC unit output voltage. It is assumed that PFC activates in normal mode and PFC stops in active standby/burst mode.

Figure 32 Active standby/burst mode sequence

Table 16 ASTBY pin threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
AS linear operation start voltage	Vas(linon)		3.0	V
AS linear operation release voltage	Vas(linoff)		2.2	V
AS mode start voltage	Vas(on)		3.2	V
AS mode release voltage	Vas(off)		2.2	V
ASTBY pin open voltage	Vastby(open)	Vin=Vc1=16V、Vsen=1V	5.4	V
ASTBY pin charging current	Iastby(chg)	Vin=Vc1=16V、Vsen=1V、ASTBY=0V	-25	uA
Burst mode start ASTBY pin voltage	Vastby(bston)		4.0	V
Burst mode release ASTBY pin voltage	Vastby(bstoff)		3.9	V
Burst pin output stop voltage	Vbst(H)		2.0	V
Burst pin output startup voltage	Vbst(L)		1.5	V
Burst pin discharging current 1	Ibst(dis)1	ASTBY<Vastby(bston/off)	400	uA
Burst pin discharging current 2 (Burst mode)	Ibst(dis)2	ASTBY>Vastby(bston/off)	0	uA
FB discharging current 1	Ifb(dis)1	Vsen=6V、ASTBY=6V	400	uA
FB discharging current 2	Ifb(dis)2	Vsen=6V、ASTBY=2V	0	uA

2.3.9 Thermal shutdown protection function (TSD function)

The MCZ5211ST features an thermal shutdown protection function, which when triggered stops LLC oscillation.

The thermal shutdown protection operation start temperature is the operation stop temperature (**TSD: 140 °C.min**). The thermal shutdown protection temperature exhibits hysteresis, and the function is canceled and returns to normal operation at the thermal shutdown protection cancel temperature when **ΔTSD** falls **40 °C** below the operation stop temperature.

Table 17 TSD function threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
Operation stop temperature	TSD		140	℃
Temperature gap between operation stop and return to normal	ΔTSD		40	℃

2.3.10 Vc1 overvoltage protection function (Vc1 OVP function)

The MCZ5211ST includes a latch stop function when the Vc1 pin overvoltage is applied. If the Vc1 pin voltage exceeds the Vc1(ovp latch) voltage of 33.0 V, latching stops. To cancel the latch stop, the Vc2 pin voltage must be set to the Vc2(latch reset) voltage of 7.0 V or less.

Table 18 Vc1 OVP function threshold values
For more information on individual ratings, refer to the characteristic specifications.

Item	Symbol	Condition	Rating	
Vc1 overvoltage protection voltage	Vc1(ovp latch)		33.0	V
Latch release voltage	Vc2(latch reset)		7.0	V

2.4 Reference

2.4.1 Operating from low input voltage

The MCZ5211ST gate output will not start during normal operation unless the Vsen pin voltage rises to the Vsen1(SS-reset) voltage of 3.00 V.

If you wish to operate the LLC from a low input voltage—for example, when evaluating a power supply—apply a voltage of at least 3.00 V or more to the Vsen pin. The Vsen pin inflow current should however be limited to around 2 mA, as the internal clamping component will conduct if the voltage exceeds approximately 12 V.

However, start up by increasing the input voltage gradually under no load conditions, as turning the input on and off in this state may cause continuous out of resonance operation, subjecting the MOSFET to a heavy load. The operation to cancel Vsen described above should be used only in cases such as power supply evaluation.

2.4.2 When Vin pin is not used

If the Vin pin is not used, either short-circuit the Vin pin to ground or leave the pin open.
Apply the Vcc supply voltage to the MCZ5211ST Vc1 pin. The capacitor between Vc2 and ground should be around 4.7 uF to 47 uF.

2.4.3 When active standby/burst mode are not used

When both active standby and burst modes are not used, short-circuit the ASTBY pin to ground. Also short-circuit the burst pin to ground.

When only burst mode is not used, short-circuit the burst pin to ground.

3.1 Input monitoring voltage section (Vsen pin)

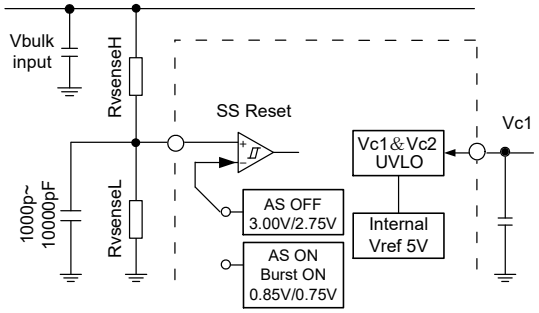
The Vsen pin threshold values are **3.00 V and 2.75 V** in normal mode, and **0.85 V and 0.75 V** in active standby mode and burst mode.

A Vsen pin sink current of 0.2 uA is required; it is recommended that the design ensures that a current of approximately 20 uA flows to avoid any sink current effects. The high-potential side Vbulk detection resistance RvsenseH should be approximately **2 MΩ**. (For a PFC output voltage of approximately 400 V)

Connect a capacitor with a capacitance of approximately 1,**000 pF to 10,000 pF** to absorb noise between the Vsen pin and ground.

Calculate the initial RvsenseL(init) value from the desired brown out protection voltage threshold Vbulkreset using **Equation (1)**, and then substitute the actual constant in **Equation (2)** to finally check the value of Vbulkreset.

In active standby mode, the Vsen threshold varies, so substitute an actual constant into **Equation (3)** to check the desired Vbulkreset(AS ON).



$$R_{VsenceL(init)} = \frac{2.75 \times R_{VsenseH}}{V_{bulkreset} - 2.75} \quad [\Omega] \qquad \cdots (1)$$

$$V_{bulkreset} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 2.75 \quad [V] \qquad \cdots (2)$$

$$V_{bulkreset(AS\,ON)} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 0.75 \quad [V] \qquad \cdots (3)$$

Figure 33 Vsen pin internal configuration

3.2 Oscillation control section (FB pin)

The LLC unit oscillation frequency is controlled by the FB pin. The FB pin determines the dead time and the initial, maximum, and minimum oscillation frequencies. As the gate on/off timing is determined by the FB pin charge/discharge timing, the capacitor and resistor connected to the FB pin should be connected as close to the IC as possible.

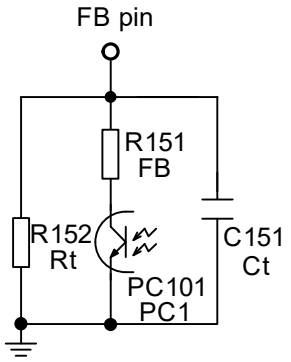


Figure 34 FB pin connection diagram

Connect the Rt resistor and FB resistor to the FB pin in addition to the Ct capacitor, as shown in Figure 34.

The capacitance of the Ct capacitor determines the dead time and initial oscillation frequency. For details, refer to Section 3.2.1.

The minimum oscillation frequency is determined by the Rt resistor, and the maximum oscillation frequency is determined by the Rt and FB resistors.

For more information on determining Rt and FB resistance, refer to Section 3.2.2 and 3.2.3.

3.2.1 Dead time and initial oscillation frequency fss adjustment (Ct capacitor adjustment)

The dead time and initial oscillation frequency fss vary depending on the capacitance of the Ct capacitor, as shown in the characteristic diagrams in Figures 35 and 36.

Select the capacitance of the Ct capacitor according to the oscillation frequency during steady operation and also the gate capacity of the MOSFET used.

As a guide for initial values, when using normal speed switching device (P15F50HP2) at a frequency of 100 kHz during normal operation, the capacitance of the Ct capacitor should be around 1,500 pF. When using high speed switching device at a frequency of 300 kHz during normal operation, the capacitance of the Ct capacitor should be around 820 pF. As the desired dead time varies based on factors such as the resonance conditions, the above values should be used as initial values and finally adjusted when mounted on the actual equipment.

When designing with the Ct capacitor in the range of 100 kHz to 500 kHz, we recommend approximately **470 pF to 2,200 pF**.

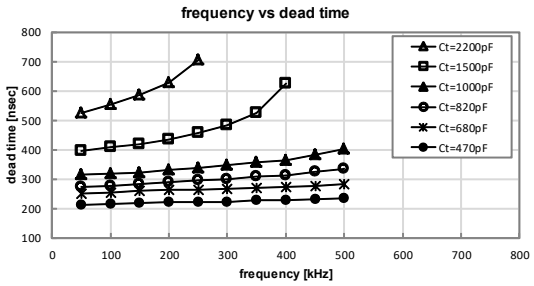


Figure 35 Dead time relationship

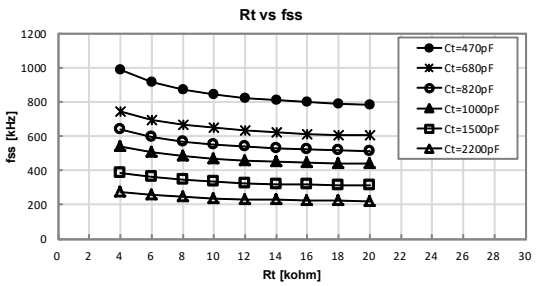


Figure 36 fss relationship

3.2.2 Minimum oscillation frequency fmin adjustment (Rt limiting resistor adjustment)

The minimum oscillation frequency fmin is determined by the Rt resistance connected between the FB pin and ground. Check the characteristic diagram in the power supply specifications for the correlation between the Rt resistance value and the oscillation frequency. Use the characteristic diagram to calculate the Rt resistance required for the desired fmin, then check fmin using **Equations (4) to (6)**.

Here, tcharge is the dead time period, and tdischarge is the period for one gate on.

After first determining the approximate values for the constants, adjust the actual oscillation frequency measured by referring to the characteristic diagram in the power supply characteristic specifications.

Note that if fmin is set too low with respect to the oscillation frequency during normal operation, the oscillation frequency will be too low for overload and load short-circuiting, causing the OCP or di/dt detection points to be reached while the FB pin voltage is at or above the FB mask voltage, resulting in OCP or di/dt masking, possibly preventing detection. When setting fmin, please check that OCP and di/dt are detected in conditions such as load short-circuiting.

$$t_{charge} = \frac{Rt \times Ct \times VFB_{(top)}}{Rt \times 9.0 \times 10^{-3} - VFB_{(top)}} - \frac{Rt \times Ct \times VFB_{(bottom)}}{Rt \times 9.0 \times 10^{-3} - VFB_{(bottom)}} \text{ [sec]} \cdots (4)$$

$$t_{discharge} = -Rt \times Ct \times \ln \frac{VFB_{(bottom)}}{VFB_{(top)}} \text{ [sec]} \cdots (5)$$

$$f_{min} = \frac{1}{2 \times \left(t_{charge} + t_{discharge} \right)} \text{ [Hz]} \cdots (6)$$

3.2.3 Maximum oscillation frequency fmax adjustment (FB limiting resistor adjustment)

The maximum oscillation frequency fmax is achieved when the photocoupler is turned on at maximum, so the FB pin resistance is determined by the value with the Rt resistor and FB resistor connected in parallel.

Let us consider here an example in which Ct is 820 pF. If the minimum oscillation frequency is approximately 150 kHz and the maximum oscillation frequency is approximately 300 kHz, the Rt resistance connected will be 10 kΩ. Since for the maximum oscillation frequency, the combined resistance will be 5 kΩ, if the Rt resistance is 10 kΩ, the FB resistance will be 10 kΩ. Finally, determine the constant after confirming the maximum and minimum oscillation frequencies on the actual equipment.

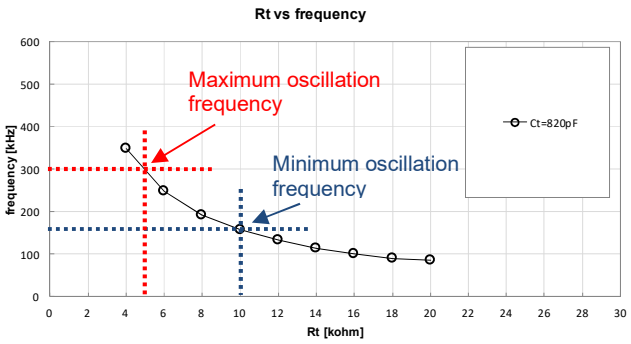


Figure 37 Maximum and minimum oscillation frequency setting example

3.3 Timer charge time adjustment for soft start and abnormality (SST pin)

The SS charging current **Isst(chg)2** to the SST pin is **30 uA** during the soft start operation. The soft start time should be designed so that an SST voltage of 1.5 V is reached, as timer charging is enabled during OCP operation when the SST voltage reaches the SS threshold **Vss value of 1.5 V** or more.

If the time until the SST voltage reaches 1.5 V from when the gate output starts at 0.6 V is tss, this can be calculated as shown in **Equation (7)**. For more information on the correlation between SST pin voltage and oscillation frequency at soft start, refer to the characteristic diagram in the characteristic specifications. If there is no OCP or other abnormality, the SST pin voltage rises to 2.1 V.

$$t_{ss} = \frac{0.9 \times C_{ss}}{30 \times 10^{-6}} \quad \text{[sec]} \quad \cdots(7)$$

Additionally, the timer charging current **Itimer(chg)1** to the SST pin on detection of di/dt for OCP1 operation and active standby operation will be **40 uA**.

Once the SST voltage has stabilized at 2.1 V, the SST pin voltage increases due to the OCP operation, and the time Ttimer taken to reach SST = 3.5 V is calculated as shown in **Equation (8)**.

$$t_{timer} = \frac{1.4 \times C_{ss}}{40 \times 10^{-6}} \quad \text{[sec]} \quad \cdots(8)$$

The charging current to the SST pin for OCP2 operation varies based on the CSO pin voltage. The timer charging current **Itimer(chg)2** when CSO ≤ 2.0 V will be **1.7 uA**. The time Ttimer taken to reach SST = 3.5 V is calculated as shown in **Equation (9)**.

$$t_{timer} = \frac{1.4 \times C_{ss}}{1.7 \times 10^{-6}} \quad \text{[sec]} \cdots(9)$$

The timer charging current **Itimer(chg)3** when CSO > 2.0 V will be **40 uA**, and the time Ttimer taken to reach SST = 3.5 V is calculated as shown in **Equation (8)**.

Additionally, the timer discharging current **Itimer(dischg)** from the SST pin will be **6.5 uA** during the intermittent operation after reaching SST = 3.5 V.

Note that the oscillation stop period during intermittent operation is canceled when the SST voltage decreases to the **Vtimer(reset) voltage of 0.40 V**. The oscillation stop period Ttimer(Stop) for intermittent operation is therefore calculated as shown in **Equation (10)**.

$$t_{timer(Stop)} = \frac{3.1 \times C_{ss}}{6.5 \times 10^{-6}} \quad \text{[sec]} \quad \cdots(10)$$

3.4 Overcurrent protection (OCP, di/dt) point adjustment (CS pin)

LLC unit overcurrent is detected by the CS pin.

The current Ipk flowing through the resonant capacitor C123 is converted into a voltage by the detection resistance R141, and the voltage divided by R143 and R144 is then detected by the CS pin.

As a CS pin current of 100 uA flows through the CS pin, it is recommended that R143 be approximately 10 Ω to 47 Ω.

Additionally, insert a filter capacitor in C141 to prevent malfunctions due to switching noise. It is recommended that the filter capacitor be approximately 0.01 uF.

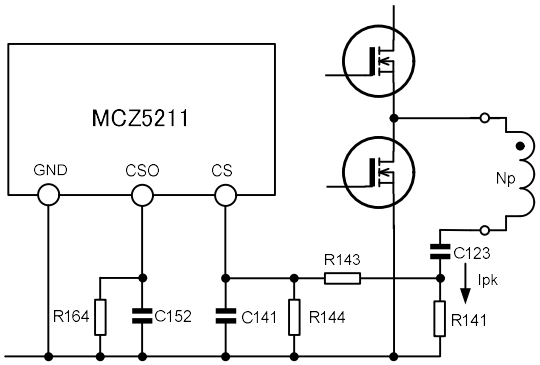


Figure 38 Overcurrent detection circuit

The overcurrent protection function OCP1 is ±0.550 V and OCP2 is ±0.350 V, so OCP2 activates first. (When SSD = 5 V)

If the resonant capacitor current is Ipk during the desired OCP2 operation, the voltage detection resistance R141 must be a constant that satisfies Equation (11). R143 and R144 are calculated using Equation (12). The R144 constant is calculated with R143 as around 10 Ω to 47 Ω. Note that the OCP2 detection threshold value is reduced to a maximum of 0.26 V if the OCP2 input voltage correction function described in 2.3.5 is used, so Equations (11) to (13) should be used for calculation with the value 0.35 suitably replaced.

Finally, check that the desired Ipk value is obtained by entering an actual constant in Equation (13).

$$\mathrm{R141} > \frac{0.35}{\mathrm{Ipk}} \qquad [\Omega] \quad \cdots \quad (11)$$

$$\mathrm{R144} = \frac{0.35 \times \mathrm{R143}}{\mathrm{Ipk} \times \mathrm{R141} - 0.35} \qquad [\Omega] \quad \cdots \quad (12)$$

$$\mathrm{I_d} = \frac{\mathrm{R143} + \mathrm{R144}}{\mathrm{R144} \times \mathrm{R141}} \times 0.35 \qquad [\mathrm{A}] \quad \cdots \quad (13)$$

Connect capacitor C152 and resistor R164 to the CSO pin. The CSO pin is charged to vary the oscillation frequency during OCP1 and OCP2 operations. See Table 5 for more information on the CSO pin charging current during OCP1 and OCP2 operations. Adjust the capacitor connected to the CSO pin after confirming the response with the actual equipment. The initial value for C152 is between 1,000 pF and 1.0 uF, and for R164 is between 10 kΩ and 100 kΩ. If you wish to latch the intermittent timer safely by narrowing the oscillation frequency earlier—for example, when the load is short-circuited—accelerate the response by setting C152 to 1,000 pF and R164 to 100 kΩ or just left open. In this case, check that the output voltage is not reduced due to OCP2 detection within the normal operating range, as the response speed is increased when OCP2 is detected.

3.5 Circuit constant settings when using active standby

Figure 39 shows an example circuit configuration when using active standby.

Active standby mode is selected when the ASTBY pin voltage is 3.2 V or higher. As burst mode is selected when the ASTBY pin voltage is 4.0 V or higher, set the ASTBY voltage for active standby mode to 3.2 V or higher and lower than 4.0 V.

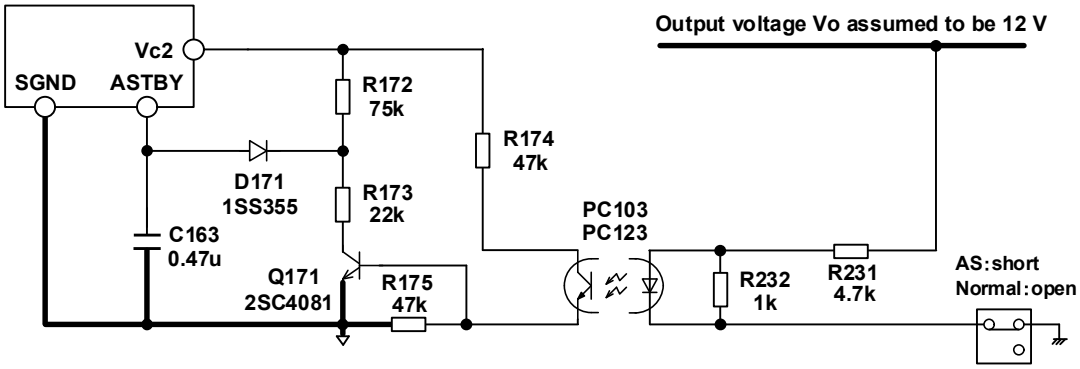


Figure 39 Active standby circuit example

Figure 39 shows an example circuit configuration for selecting active standby mode by short-circuiting the secondary side switch to ground. Short-circuiting the secondary side switch to ground energizes the PC103 photocoupler and turns on Q171. The voltage corresponding to the voltage determined by the divided resistance of R172 and R173 added to the Vf component of D171 is therefore generated as the ASTBY pin voltage. As the forward current flowing through D171 is 1 mA or less, check the diode Vf at this point.

If the D171 reverse current is large, the ASTBY voltage may increase even in normal mode. A diode with a low reverse current not exceeding 1 uA should therefore be selected for D171.

3.6 Circuit constant settings when using burst mode

Figures 40 and 41 show examples of circuit configurations when using burst mode. In both Figure 40 and 41 it is assumed that 5 V is output using DC/DC from the 12 V output voltage.

The lower limit of the 12 V output voltage in burst mode is determined by the resistances of R223 and R224. The output voltage lower limit will be 7.84 V when the IC202 reference voltage is 2.5 V, R223 is 47 kΩ, and R224 is 22 kΩ.

The burst pin discharging current during normal active standby will be 400 uA, so if the resistance values for R159 and R164 are too low, the burst pin voltage will rise, possibly causing intermittent operation. R159 should be approximately 15 kΩ, and the R164 resistance should be used to adjust the burst cycle. R164 was set so that the burst pin voltage is at least 1.5 V when the auxiliary winding voltage is around 10 V, taking into account Vc2 UVLO.

R165 and C157 were determined taking into account factors such as the burst cycle. A diode with a low reverse current should be selected for D163 in the same way as for D171 in Section 3.5.

R166 shown in Figure 40 must not exceed 1.8 V in normal mode. For example, if R166 is 47 kΩ with the coupler completely short-circuited, the ASTBY charging current will be 25 uA, so the ASTBY pin voltage is calculated to rise up to 1.18 V. Note that if the load is increased in burst mode, the number of PC102 turn-on cycles increases, and the ASTBY pin takes longer to discharge. However, if the discharging current is larger than the ASTBY charging current, burst mode may be canceled due to the ASTBY pin voltage dropping. If there is a possibility of the burst cycle becoming shorter, use the circuit configuration shown in Figure 41.

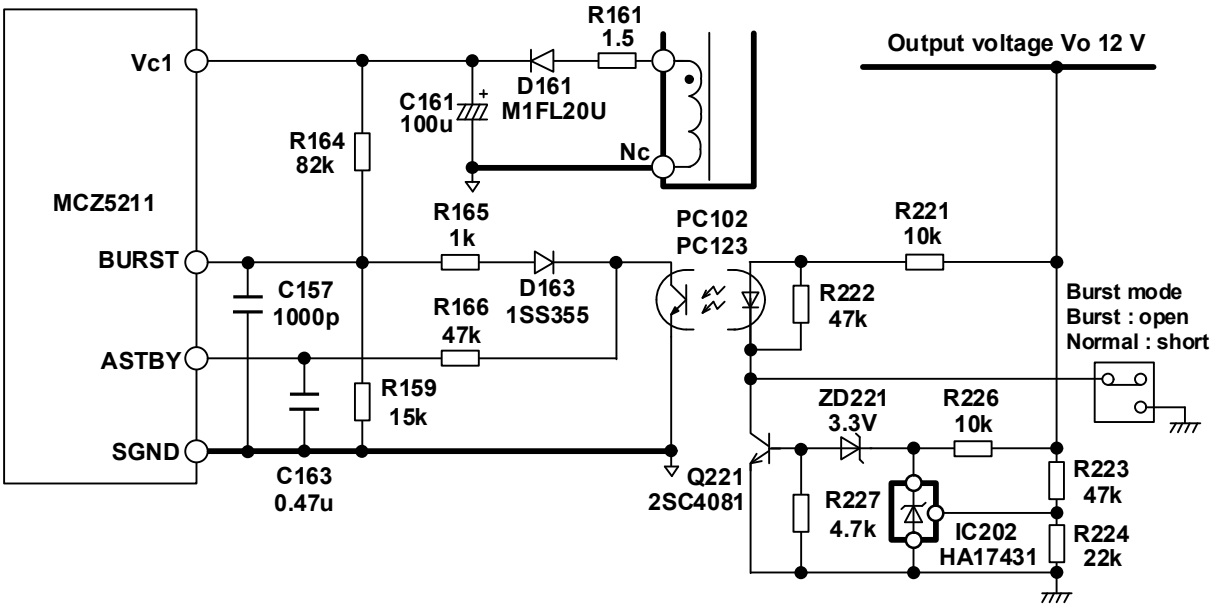


Figure 40 Active standby circuit example (using one coupler)

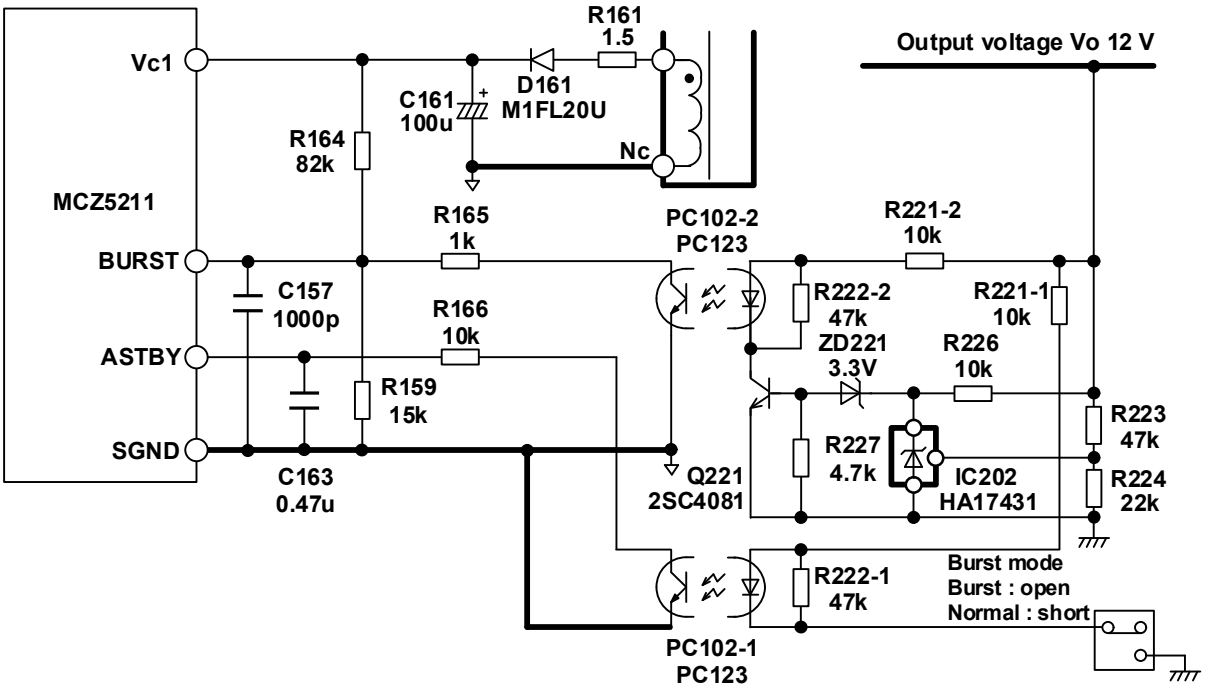


Figure 41 Active standby circuit example (using two couplers)

4 IC Peripheral Pattern Layout Precautions

4.1 IC peripheral pattern layout precautions

The pattern layout of the switching power supply board will affect the power supply characteristics. The MCZ5211ST switches high voltages and large currents, so great care is required when laying out the circuit pattern.

To minimize issues such as noise due to pattern inductance components, it is important to design the main circuit to ensure patterns are as thick and short as possible. Also be sure to wire the control system pattern to eliminate effects from electric and magnetic fields.

Please refer to the precaution points set out here for each major item.

① Main current path wiring

Connect the power system ground separated from the main current line returning to the input capacitor from the low-side MOSFET source to the IC ground. Also connect the signal system ground and power system ground closest to the IC ground pin, keeping the signal system ground separate from the power system ground.

② Signal line wiring

Signal system line components such as capacitors and resistors (e.g., FB pin, CS pin, Vc1/2 pins) should be connected as close to the IC as possible to prevent malfunctions.

If the patterns between the FB pin photocouplers and the return from the photocouplers are close to the pattern for the high-voltage switching line (e.g., resonant capacitor), the FB pin voltage may fluctuate, affecting the high-side/low-side gate output. Arrange the patterns as far as possible from high-voltage lines, resonant capacitors, and transformers.

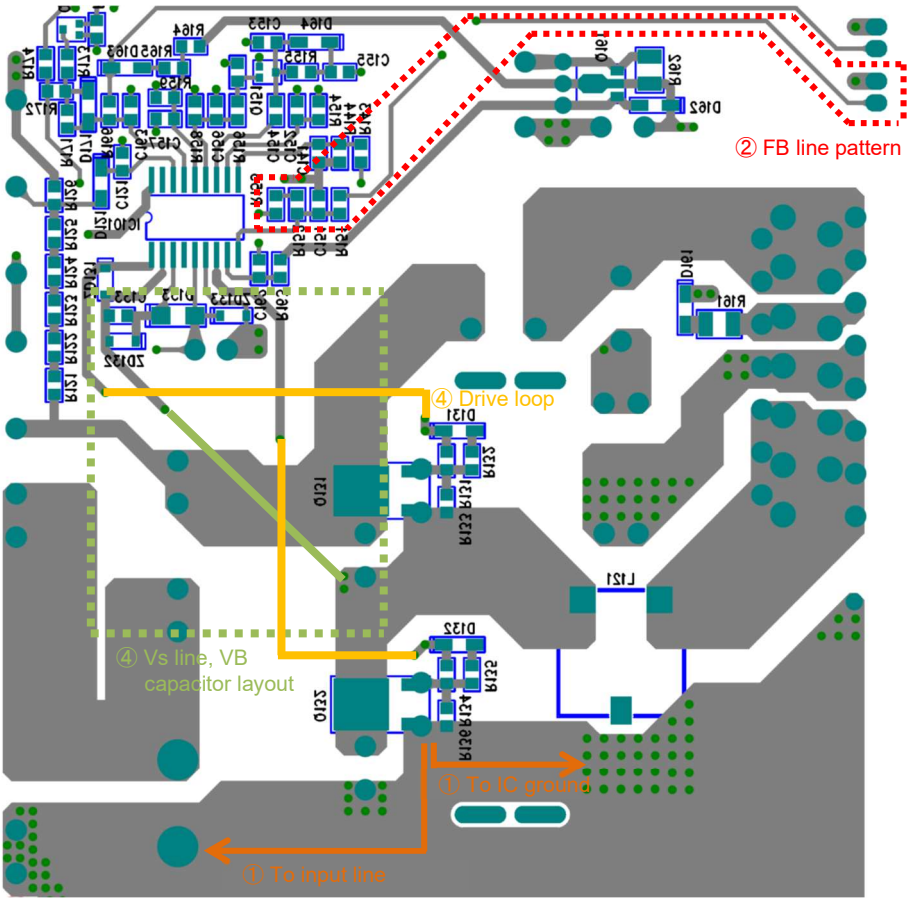
The CS pin is the pin used for overcurrent detection. Fluctuations in the CS pin voltage may result in malfunctions if the pattern between the CS pin and the detection resistance is close to high-voltage switching lines. As with the FB pin, configure the patterns as far as possible from high-voltage lines, resonant capacitors, and transformers.

③ Gate output line wiring

The gate charging/discharging current has a sharp spike shape. The surge voltage attributable to the parasitic L/C of the pattern and components may result in unstable IC function. Keep the drive loop system away from the signal system ground.

④ High-voltage line wiring

Position the bootstrap smoothing capacitor as close as possible to the IC. Connect the VS line connected to the high-side MOSFET source directly. Keep separate from the main switching current line.



【Precautions when measuring waveforms】

(a) Measuring MOSFET current

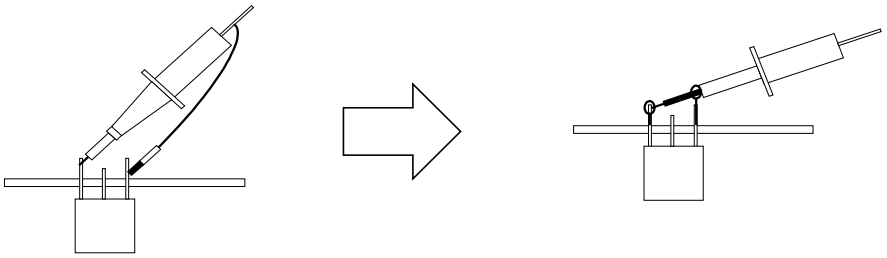
To minimize the effects of the parasitic impedance of the lead wire, use wire with a withstand voltage of at least 500 V. Connect using the shortest possible wiring routes. Additionally, use a DC probe.

(b) Measuring high potential side voltage

Carefully note the probe withstand voltage. Components such as the LLC MOSFET, primary side resonant capacitors, and transformers are high-voltage components. Use a calibrated differential probe when measuring floating sections since the LLC high-side MOS, VGH, VS, and VB pins are floating circuits.

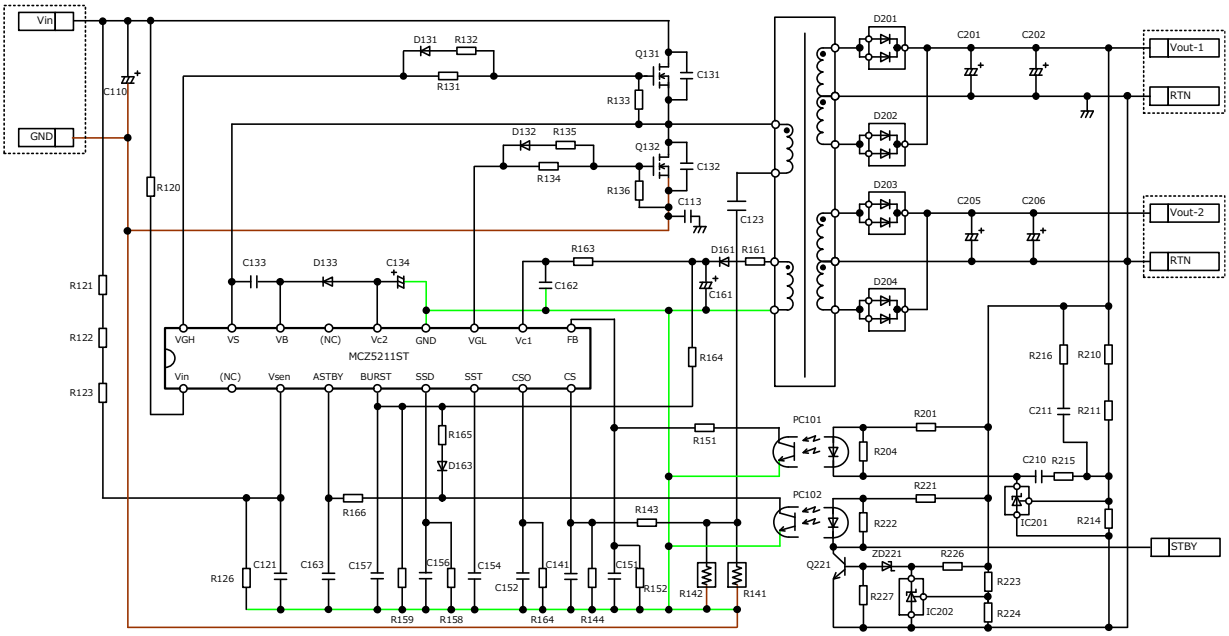
(c) Measuring low potential side

When measuring low-voltage/high-frequency pins such as the FB pin, switching noise may be superimposed depending on how the probe is grounded, resulting in waveforms different from the actual waveform. If the surge voltage component affects measurements, do not use a ground lead for the voltage probe. Instead, measure the ground directly by positioning a pin at the measurement point as shown in the diagram below. In particular, the oscillation frequency of the LLC unit is determined between the FB and ground pins. Take precautions over the ground connection when measuring with the probe to eliminate effects attributable to the probe connection.



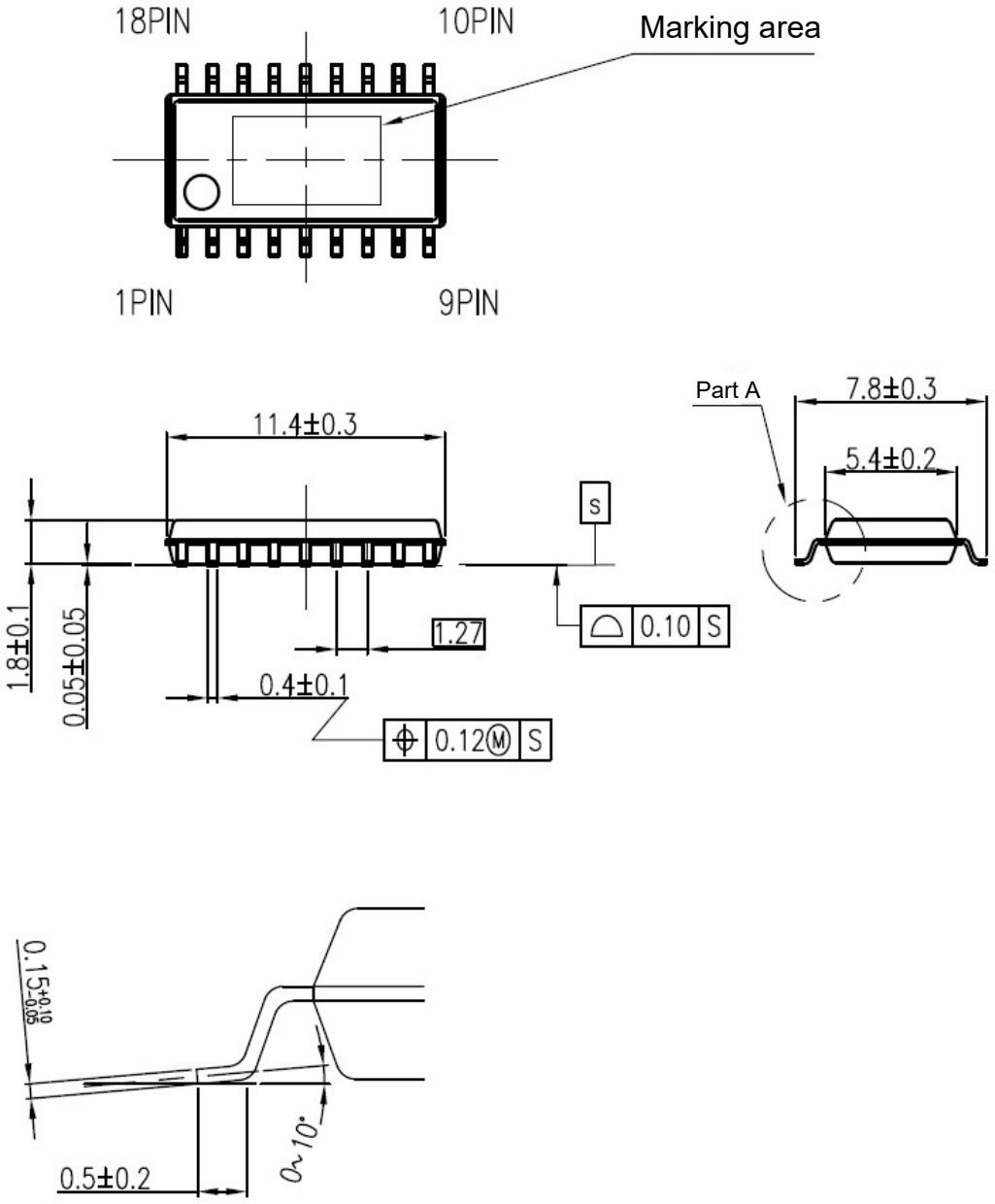
5 Circuit Examples

5.1 Typical circuit diagram



6 External Dimension Diagrams
(For official dimensions, refer to the delivery specifications.)

6.1 SOP18 (MCZ5211ST)



Detailed schematic diagram of part A (12:1)

Notes: